15-W Filter-Free Stereo Class-D Audio Power Amplifier with SpeakerGuard™

Check for Samples: TPA3110D2-Q1

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C2
- 15-W/ch Into 8-Ω Loads at 10% THD+N From a 16-V Supply
- 10-W/ch Into 8-Ω Loads at 10% THD+N From a 13-V Supply
- 30-W Into a 4-Ω Mono Load at 10% THD+N From a 16-V Supply
- 90% Efficient Class-D Operation Eliminates Need for Heat Sinks
- Wide Supply Voltage Range Allows Operation from 8 V to 26 V
- Filter-Free Operation
- SpeakerGuard Protection Circuitry Includes Adjustable Power Limiter Plus DC Protection
- Flow Through Pin Out Facilitates Easy Board Layout
- Robust Pin-to-Pin Short-Circuit Protection and Thermal Protection with Auto Recovery Option
- Excellent THD+N and Pop-Free Performance
- Four Selectable Fixed Gain Settings
- Differential Inputs

APPLICATIONS

- Automotive Noise Generation for HEV/EV
- Automotive Emergency Call Systems
- PC and Laptop Mono Applications
- Consumer Audio Electronics

DESCRIPTION

The TPA3110D2-Q1 is a 15-W (per channel) efficient, Class-D audio power amplifier for driving bridged-tied stereo speakers. Advanced EMI suppression technology enables the use of inexpensive ferrite bead filters at the outputs while meeting EMC requirements. SpeakerGuard protection circuitry includes an adjustable power limiter and a DC detection circuit. The adjustable power limiter allows the user to set a virtual voltage rail lower than the chip supply to limit the amount of current through the speaker. The DC detect circuit measures the frequency and amplitude of the PWM signal and shuts off the output stage if the input capacitors are damaged or shorts exist on the inputs.

The TPA3110D2-Q1 can drive stereo speakers as low as 4 Ω. The high efficiency of the TPA3110D2-Q1, 90%, eliminates the need for an external heat sink when playing music.

The outputs are also fully protected against shorts to GND, VCC, and output-to-output. The short-circuit protection and thermal protection includes an auto-recovery feature.

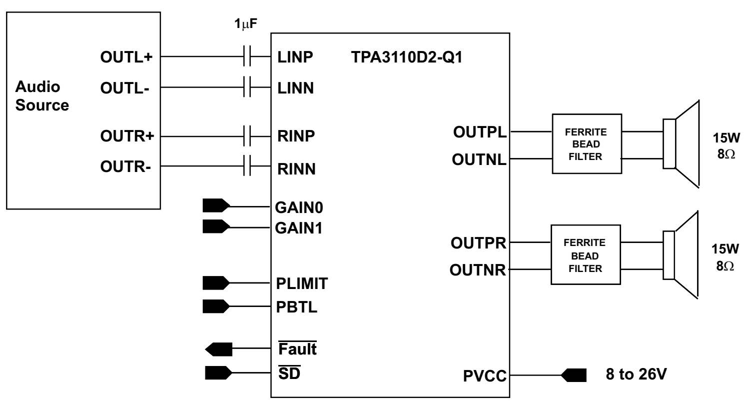


Figure 1. TPA3110D2-Q1 Simplified Application Schematic

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SpeakerGuard, PowerPAD are trademarks of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	TPA3110D2QPWPRQ1	TPA3110Q1

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)[(1)]

			VALUE		UNIT
			MIN	MAX	
V_{CC}	Supply voltage	AVCC, PVCC	–0.3	30	V
V_I	Interface pin voltage	$\overline{SD}$, GAIN0, GAIN1, PBTL, $\overline{FAULT}$ [(2)]	–0.3	V_{CC} + 0.3	V
				< 10	V/ms
		PLIMIT	–0.3	GVDD + 0.3	V
		RINN, RINP, LINN, LINP	–0.3	6.3	V
	Continuous total power dissipation		See the Thermal Information Table		
T_A	Operating free-air temperature range		–40	125	°C
T_J	Operating junction temperature range[(3)]		–40	150	°C
T_{stg}	Storage temperature range		–65	150	°C
R_L	Minimum load resistance	BTL: PVCC > 15 V		4.8	
		BTL: PVCC ≤ 15 V		3.2	
		PBTL		3.2	
ESD	Electrostatic discharge	Human-body model (HBM) AEC-Q100 classification level H2		4	kV
		Charged-device model (CDM) AEC-Q100 classification level C2		250	V
		Machine model (MM) per JESD22-A115		200	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operations of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The voltage slew rate of these pins must be restricted to no more than 10 V/ms. For higher slew rates, use a 100-kΩ resistor in series with the pins, per application note SLUA626.
(3) The TPA3110D2-Q1 incorporates an exposed thermal pad on the underside of the chip. This acts as a heatsink, and it must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in the device going into thermal protection shutdown. See TI Technical Brief SLMA002 for more information about using the TSSOP thermal pad.

THERMAL INFORMATION

THERMAL METRIC[(1)(2)]		TPA3110D2-Q1	UNIT
		PWP (28 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	30.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	33.5	
θ_{JB}	Junction-to-board thermal resistance	17.5	
ψ_{JT}	Junction-to-top characterization parameter	0.9	
ψ_{JB}	Junction-to-board characterization parameter	7.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	PVCC, AVCC	8	26	V
V_{IH}	High-level input voltage	$\overline{SD}$, GAIN0, GAIN1, PBTL	2		V
V_{IL}	Low-level input voltage	$\overline{SD}$, GAIN0, GAIN1, PBTL		0.8	V
V_{OL}	Low-level output voltage	$\overline{FAULT}$, $R_{PULL-UP}$ = 100k, V_{CC} = 26 V		0.8	V
I_{IH}	High-level input current	$\overline{SD}$, GAIN0, GAIN1, PBTL, V_I = 2 V, V_{CC} = 18 V		50	µA
I_{IL}	Low-level input current	$\overline{SD}$, GAIN0, GAIN1, PBTL, V_I = 0.8 V, V_{CC} = 18 V		5	µA
T_A	Operating free-air temperature		–40	125	°C

DC CHARACTERISTICS

T_A = –40°C to 125°C, V_{CC} = 24 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\| V_{OS} \|$	Class-D output offset voltage (measured differentially)	V_I = 0 V, Gain = 36 dB			1.5	15	mV
I_{CC}	Quiescent supply current	$\overline{SD}$ = 2 V, no load, PV_{CC} = 24 V			32	50	mA
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	$\overline{SD}$ = 0.8 V, no load, PV_{CC} = 24 V			250	400	µA
$r_{DS(on)}$	Drain-source on-state resistance	V_{CC} = 12 V, I_O = 500 mA, T_J = 25°C	High side		240		mΩ
			Low side		240		
G	Gain	GAIN1 = 0.8 V	GAIN0 = 0.8 V	19	20	21	dB
			GAIN0 = 2 V	25	26	27	
		GAIN1 = 2 V	GAIN0 = 0.8 V	31	32	33	dB
			GAIN0 = 2 V	35	36	37	
t_{on}	Turn-on time	$\overline{SD}$ = 2 V			14		ms
t_{OFF}	Turn-off time	$\overline{SD}$ = 0.8 V			2		µs
GVDD	Gate drive supply	I_{GVDD} = 100 µA		6.4	6.9	7.4	V
t_{DCDET}	DC detect time	$V_{(RINN)}$ = 6 V, VRINP = 0 V			420		ms

DC CHARACTERISTICS

T_A = –40°C to 125°C, V_{CC} = 12 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\| V_{OS} \|$	Class-D output offset voltage (measured differentially)	V_I = 0 V, Gain = 36 dB			1.5	15	mV
I_{CC}	Quiescent supply current	$\overline{SD}$ = 2 V, no load, PV_{CC} = 12 V			20	35	mA
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	$\overline{SD}$ = 0.8 V, no load, PV_{CC} = 12 V			200		µA
$r_{DS(on)}$	Drain-source on-state resistance	V_{CC} = 12 V, I_O = 500 mA, T_J = 25°C	High side		240		mΩ
			Low side		240		
G	Gain	GAIN1 = 0.8 V	GAIN0 = 0.8 V	19	20	21	dB
			GAIN0 = 2 V	25	26	27	
		GAIN1 = 2 V	GAIN0 = 0.8 V	31	32	33	dB
			GAIN0 = 2 V	35	36	37	
t_{ON}	Turn-on time	$\overline{SD}$ = 2 V			14		ms
t_{OFF}	Turn-off time	$\overline{SD}$ = 0.8 V			2		µs
GVDD	Gate drive supply	I_{GVDD} = 2 mA		6.4	6.9	7.4	V
V_O	Output voltage maximum under PLIMIT control	$V_{(PLIMIT)}$ = 2 V; V_I = 1 V_{RMS}		6.75	7.90	8.75	V

AC CHARACTERISTICS

T_A = –40°C to 125°C, V_{CC} = 24 V, R_L = 8 Ω (unless otherwise noted)

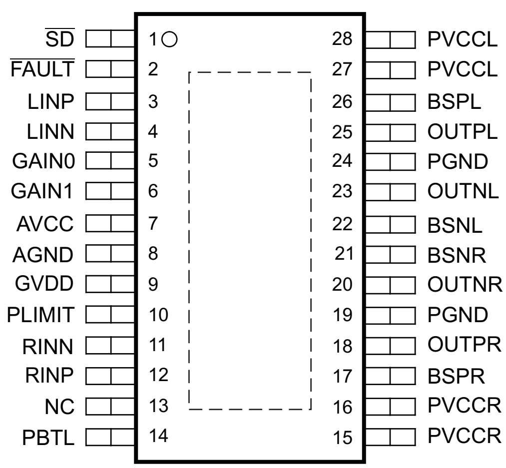
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
K_{SVR}	Power supply ripple rejection	200 mV_{PP} ripple at 1 kHz, Gain = 20 dB, inputs AC-coupled to AGND		–70		dB
P_O	Continuous output power	THD+N = 10%, f = 1 kHz, V_{CC} = 16 V		15		W
THD+N	Total harmonic distortion + noise	V_{CC} = 16 V, f = 1 kHz, P_O = 7.5 W (half-power)		0.1		%
V_n	Output integrated noise	20 Hz to 22 kHz, A-weighted filter, Gain = 20 dB		65		µV
				–80		dBV
	Crosstalk	V_O = 1 V_{RMS}, Gain = 20 dB, f = 1 kHz		–100		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1 kHz, Gain = 20 dB, A-weighted		102		dB
f_{OSC}	Oscillator frequency		250	310	350	kHz
	Thermal trip point			150		°C
	Thermal hysteresis			15		°C

AC CHARACTERISTICS

T_A = –40°C to 125°C, V_{CC} = 12 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
K_{SVR}	Supply ripple rejection	200 mV_{PP} ripple from 20 Hz–1 kHz, Gain = 20 dB, inputs AC-coupled to AGND		–70		dB
P_O	Continuous output power	THD+N = 10%, f = 1 kHz; V_{CC} = 13 V		10		W
THD+N	Total harmonic distortion + noise	R_L = 8 Ω, f = 1 kHz, P_O = 5 W (half-power)		0.06		%
V_n	Output integrated noise	20 Hz to 22 kHz, A-weighted filter, Gain = 20 dB		65		µV
				–80		dBV
	Crosstalk	P_o = 1 W, Gain = 20 dB, f = 1 kHz		–100		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1 kHz, Gain = 20 dB, A-weighted		102		dB
f_{OSC}	Oscillator frequency		250	310	350	kHz
	Thermal trip point			150		°C
	Thermal hysteresis			15		°C

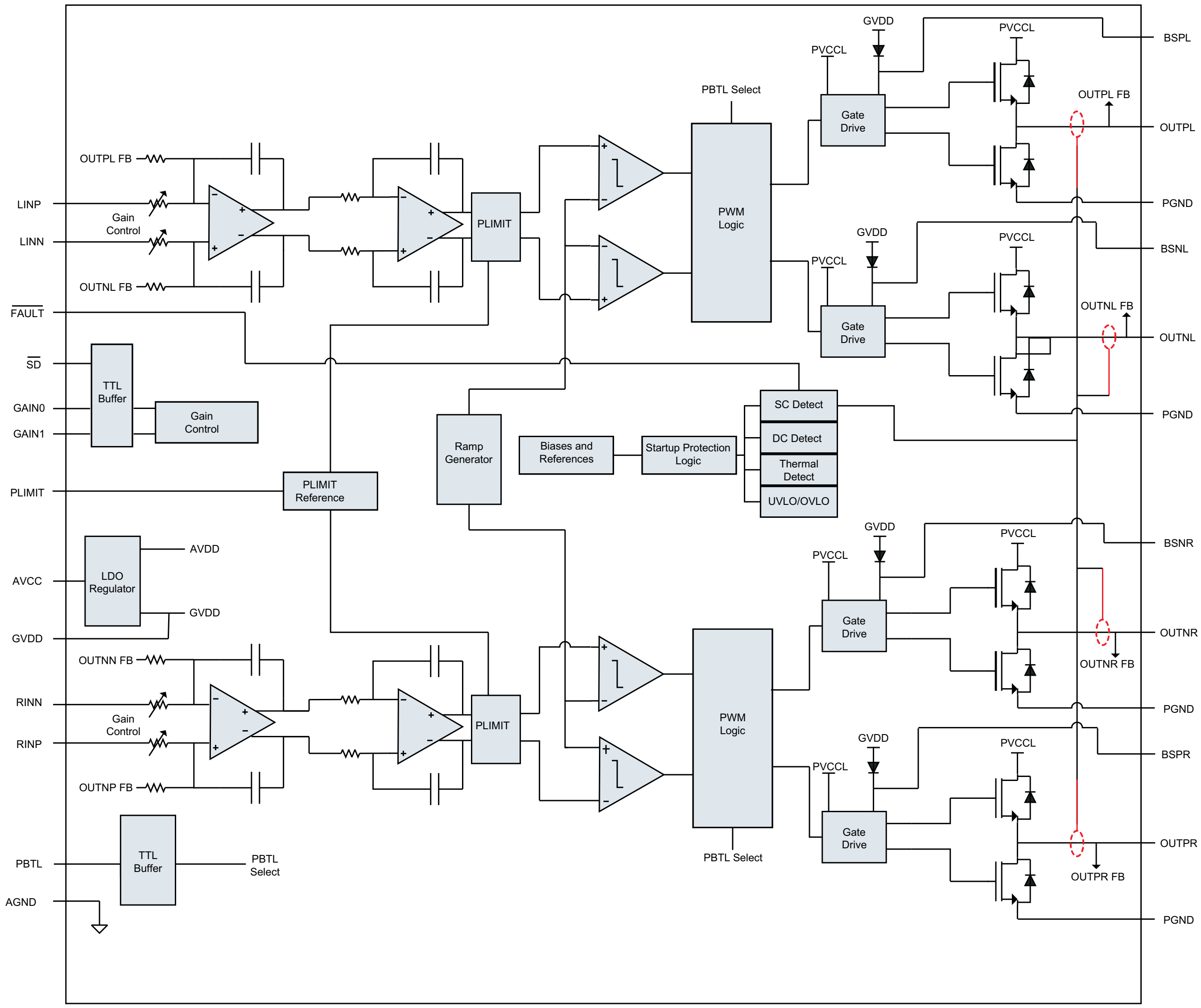
PWP (TSSOP) PACKAGE
(TOP VIEW)



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{\text{SD}}$	1	I	Shutdown logic input for audio amp (LOW = outputs Hi-Z, HIGH = outputs enabled), TTL logic levels with compliance to AVCC.
$\overline{\text{FAULT}}$	2	O	Open drain output used to display short circuit or DC detect fault status. Voltage compliant to AVCC. Short circuit faults can be set to auto-recovery by connecting $\overline{\text{FAULT}}$ pin to $\overline{\text{SD}}$ pin. Otherwise, both short circuit faults and DC detect faults must be reset by cycling PVCC.
LINP	3	I	Positive audio input for left channel, biased at 3 V.
LINN	4	I	Negative audio input for left channel, biased at 3 V.
GAIN0	5	I	Gain select least significant bit, TTL logic levels with compliance to AVCC.
GAIN1	6	I	Gain select most significant bit, TTL logic levels with compliance to AVCC.
AVCC	7	P	Analog supply
AGND	8		Analog signal ground, connect to the thermal pad.
GVDD	9	O	High-side FET gate drive supply. The nominal voltage is 7 V. GVDD should also be used as a supply for the PLIMIT function.
PLIMIT	10	I	Power limit level adjust. Connect a resistor divider from GVDD to GND to set power limit. Connect directly to GVDD for no power limit.
RINN	11	I	Negative audio input for right channel, biased at 3 V.
RINP	12	I	Positive audio input for right channel, biased at 3 V.
NC	13		Not connected
PBTL	14	I	Parallel BTL mode switch
PVCCR	15	P	Power supply for right channel H-bridge. Right channel and left channel power supply inputs are connect internally.
PVCCR	16	P	Power supply for right channel H-bridge. Right channel and left channel power supply inputs are connect internally.
BSPR	17	I	Bootstrap I/O for right channel, positive high-side FET
OUTPR	18	O	Class-D H-bridge positive output for right channel
PGND	19		Power ground for the H-bridges
OUTNR	20	O	Class-D H-bridge negative output for right channel
BSNR	21	I	Bootstrap I/O for right channel, negative high-side FET
BSNL	22	I	Bootstrap I/O for left channel, negative high-side FET
OUTNL	23	O	Class-D H-bridge negative output for left channel
PGND	24		Power ground for the H-bridges
OUTPL	25	O	Class-D H-bridge positive output for left channel
BSPL	26	I	Bootstrap I/O for left channel, positive high-side FET
PVCCL	27	P	Power supply for left channel H-bridge. Right channel and left channel power supply inputs are connect internally.
PVCCL	28	P	Power supply for left channel H-bridge. Right channel and left channel power supply inputs are connect internally.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

All measurements taken at 1 kHz, unless otherwise noted. The TPA3110D2-Q1 EVM (which is available at ti.com) made the measurements.

TOTAL HARMONIC DISTORTION vs FREQUENCY (BTL)

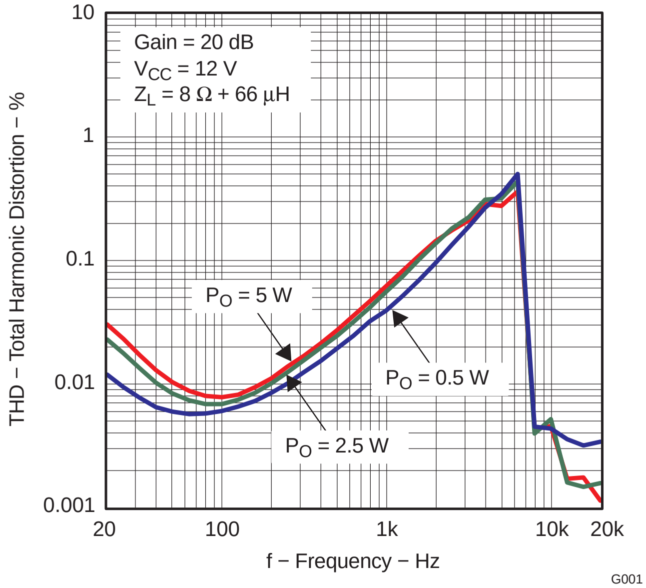


Figure 2.

TOTAL HARMONIC DISTORTION vs FREQUENCY (BTL)

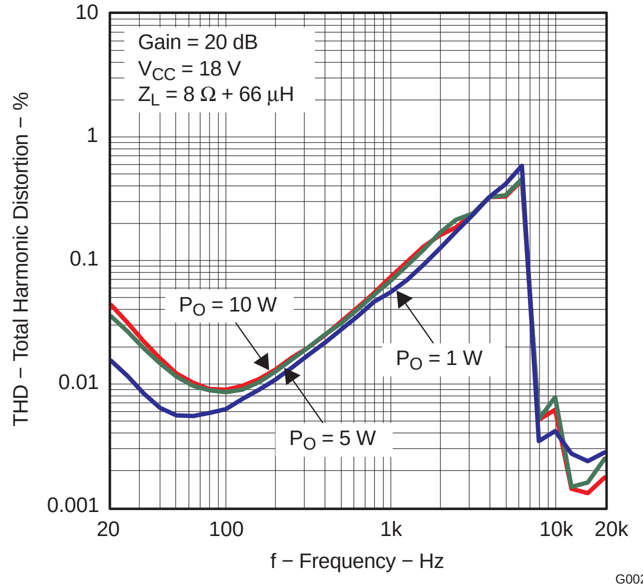


Figure 3.

TOTAL HARMONIC DISTORTION vs FREQUENCY (BTL)

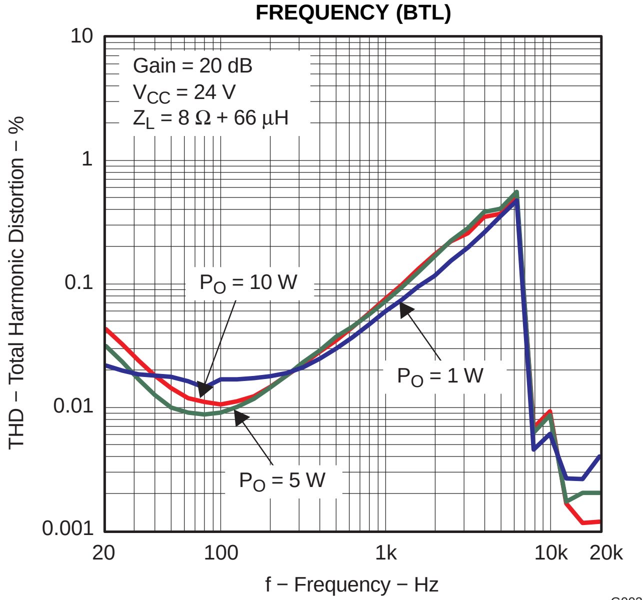


Figure 4.

TOTAL HARMONIC DISTORTION vs FREQUENCY (BTL)

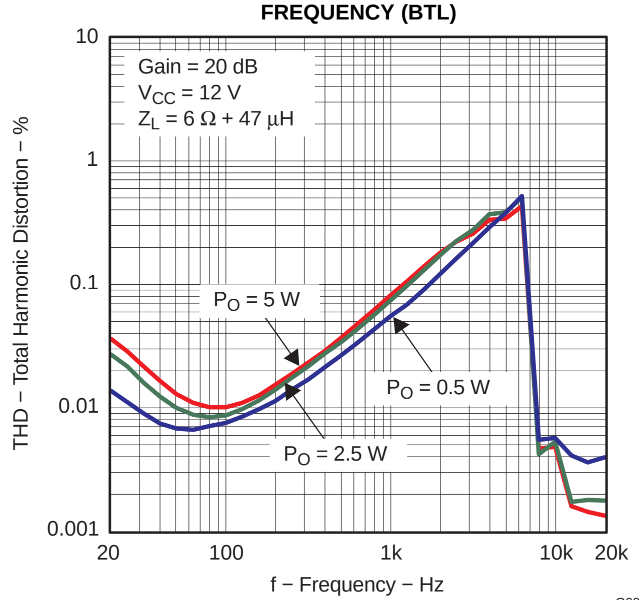


Figure 5.

TYPICAL CHARACTERISTICS (continued)

All measurements taken at 1 kHz, unless otherwise noted. The TPA3110D2-Q1 EVM (which is available at ti.com) made the measurements.

TOTAL HARMONIC DISTORTION vs FREQUENCY (BTL)

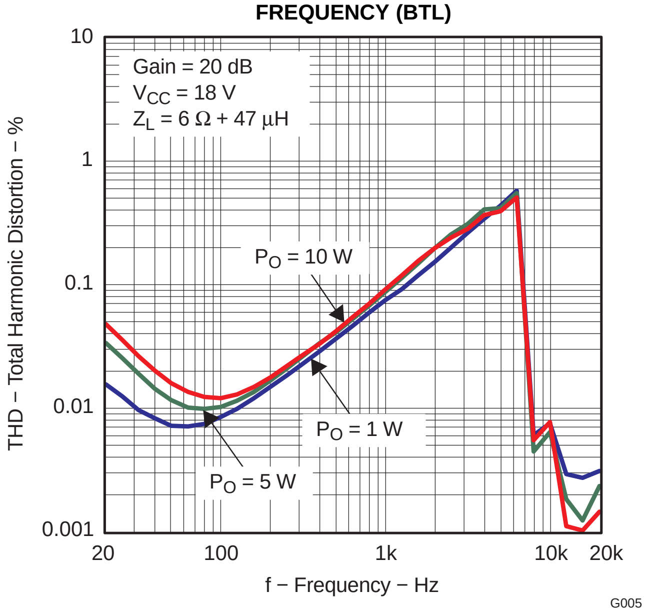


Figure 6.

TOTAL HARMONIC DISTORTION vs FREQUENCY (BTL)

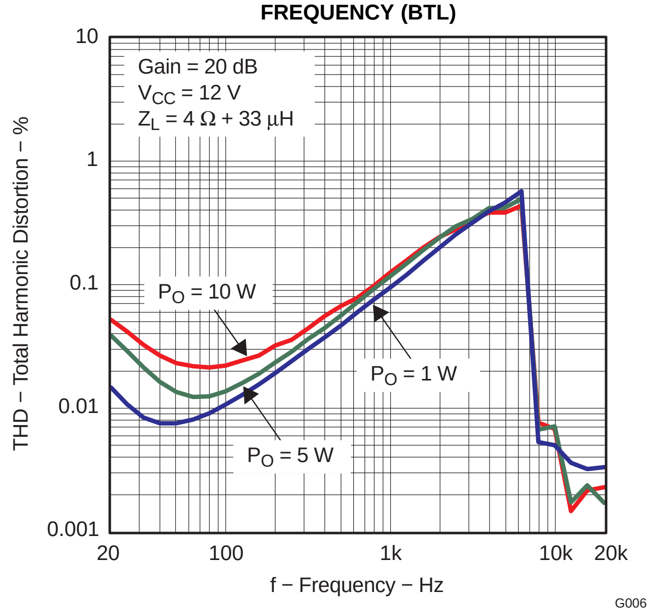


Figure 7.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER (BTL)

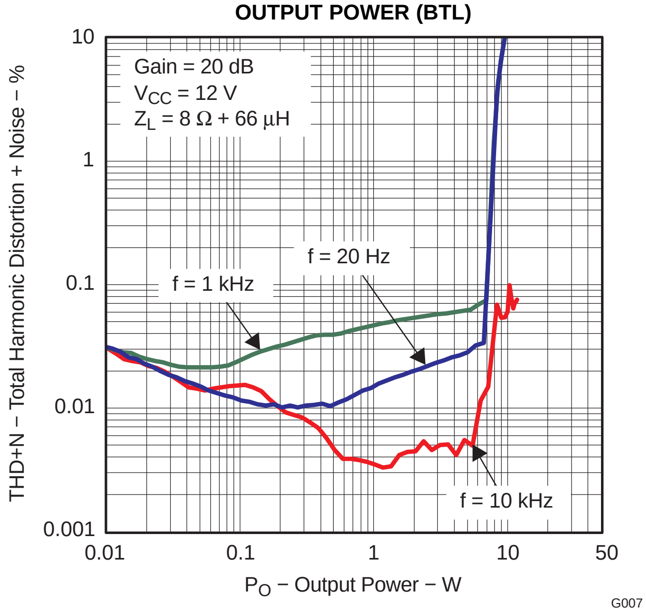


Figure 8.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER (BTL)

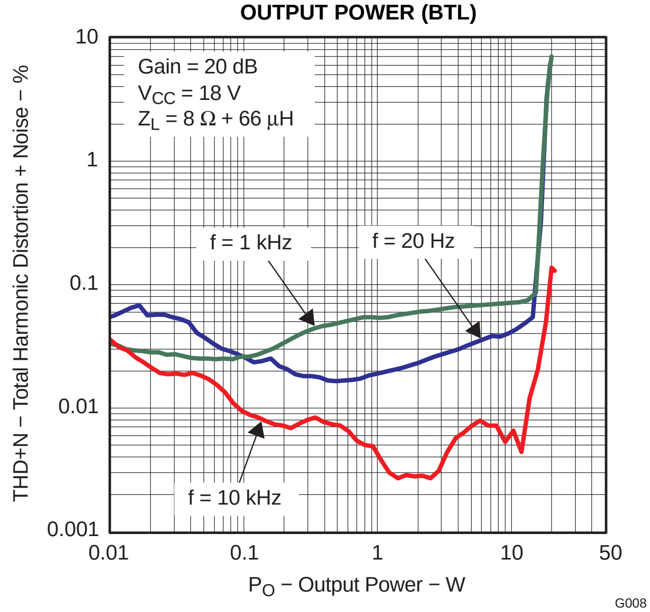


Figure 9.

TYPICAL CHARACTERISTICS (continued)

All measurements taken at 1 kHz, unless otherwise noted. The TPA3110D2-Q1 EVM (which is available at ti.com) made the measurements.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER (BTL)

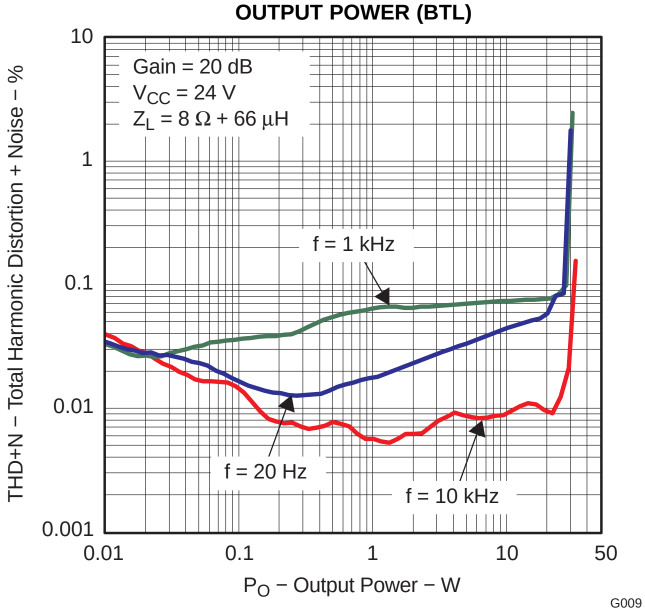


Figure 10.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER (BTL)

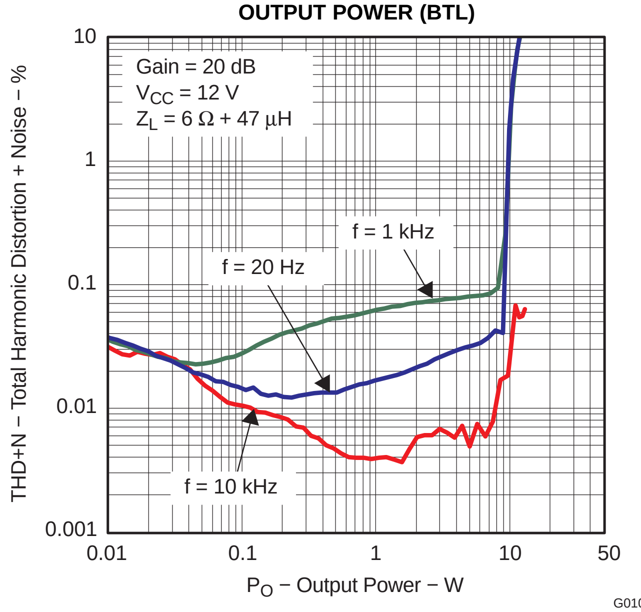


Figure 11.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER (BTL)

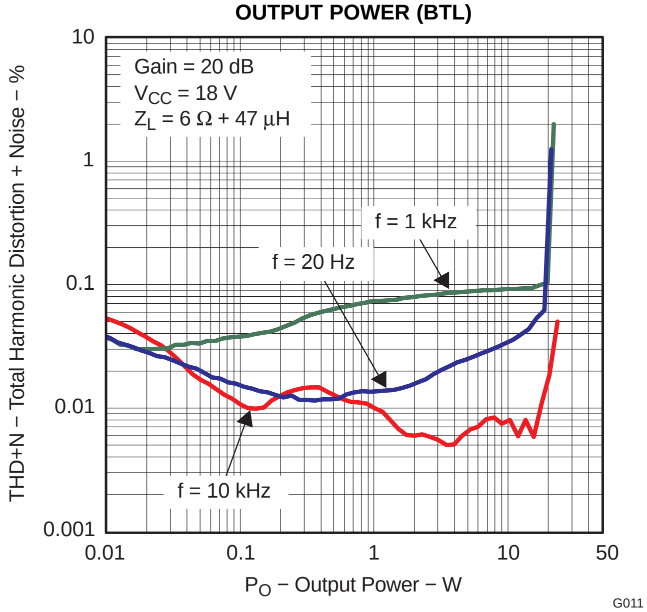


Figure 12.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER (BTL)

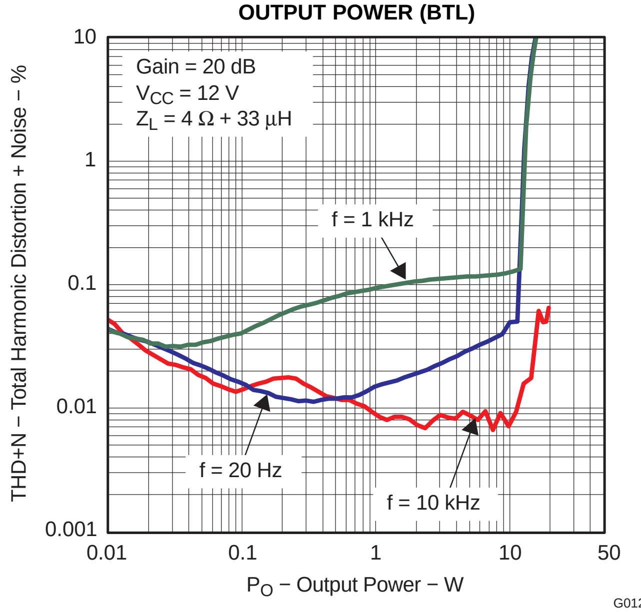


Figure 13.

TYPICAL CHARACTERISTICS (continued)

All measurements taken at 1 kHz, unless otherwise noted. The TPA3110D2-Q1 EVM (which is available at ti.com) made the measurements.

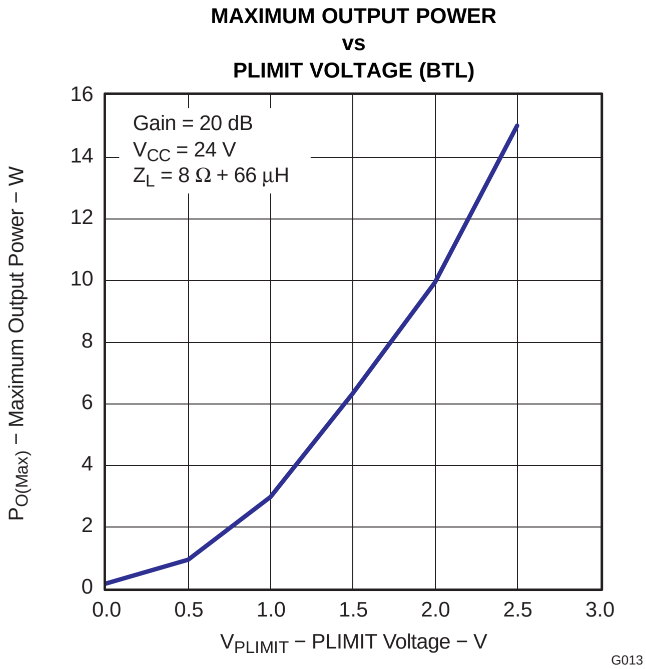
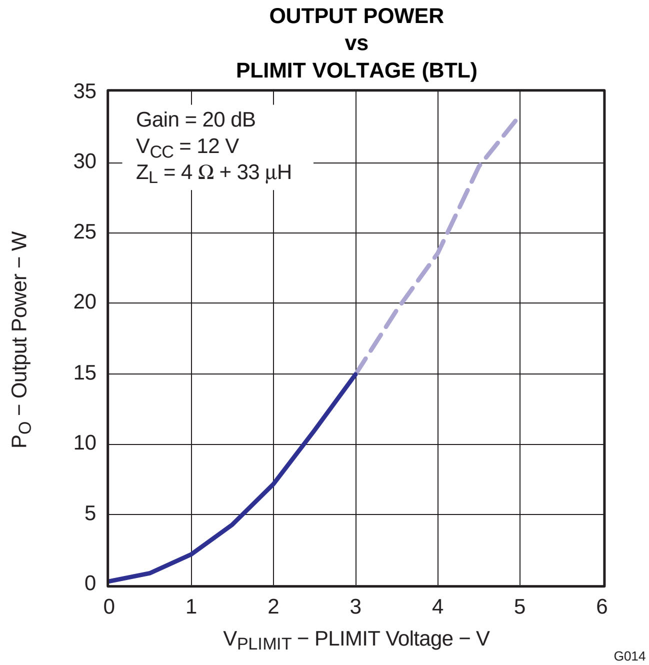


Figure 14.



Note: Dashed lines represent thermally limited regions.

Figure 15.

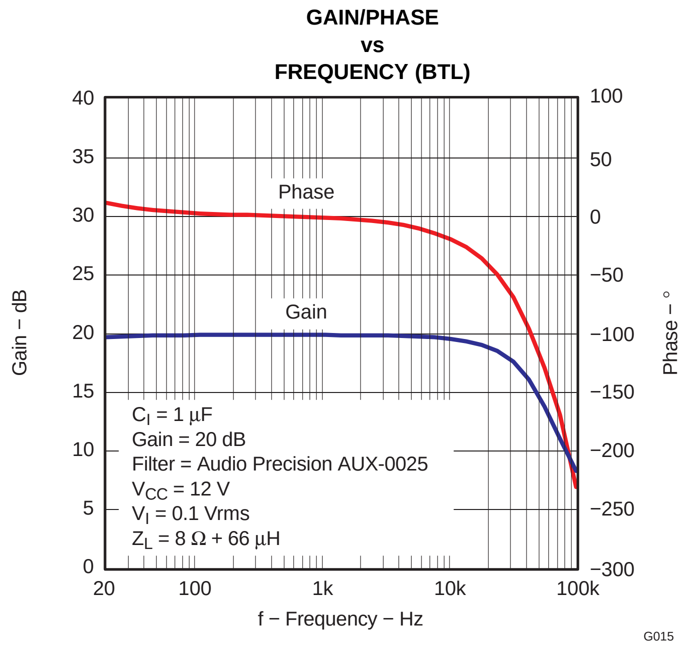
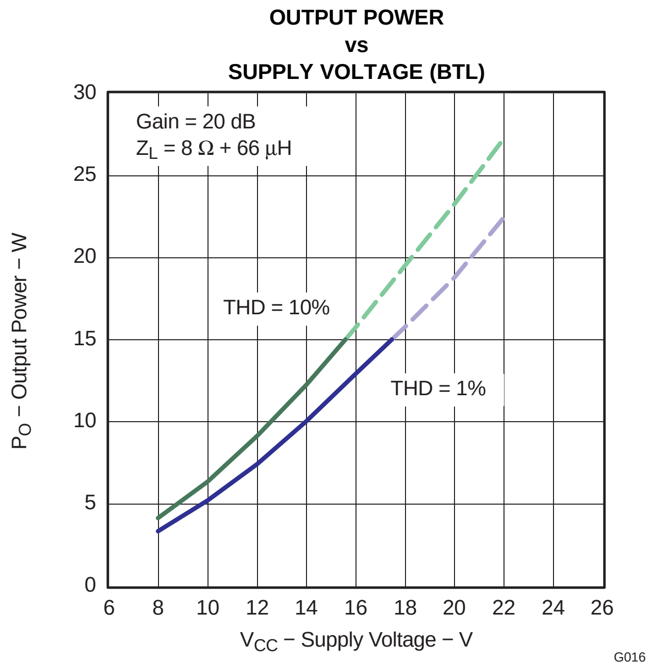


Figure 16.

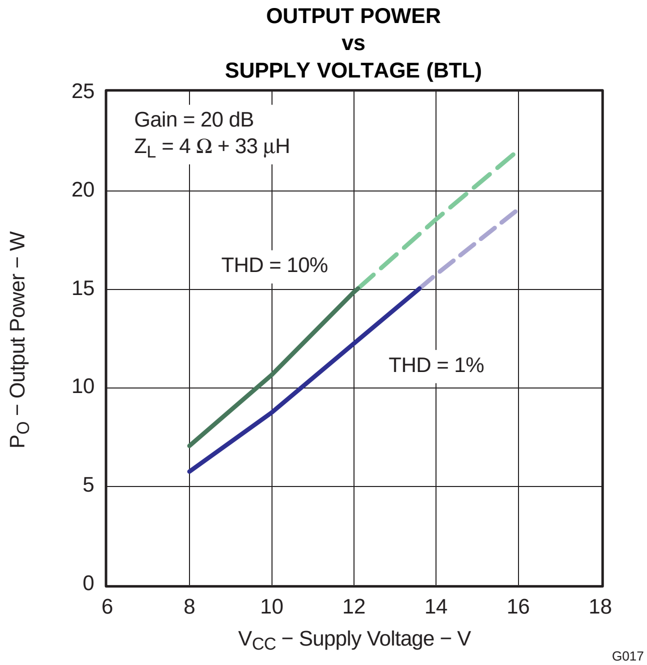


Note: Dashed lines represent thermally limited regions.

Figure 17.

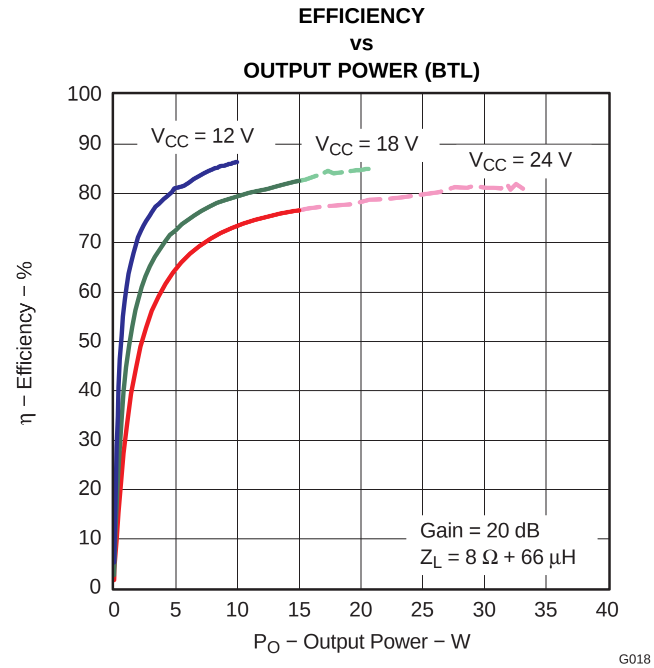
TYPICAL CHARACTERISTICS (continued)

All measurements taken at 1 kHz, unless otherwise noted. The TPA3110D2-Q1 EVM (which is available at ti.com) made the measurements.



Note: Dashed lines represent thermally limited regions.

Figure 18.



Note: Dashed lines represent thermally limited regions.

Figure 19.

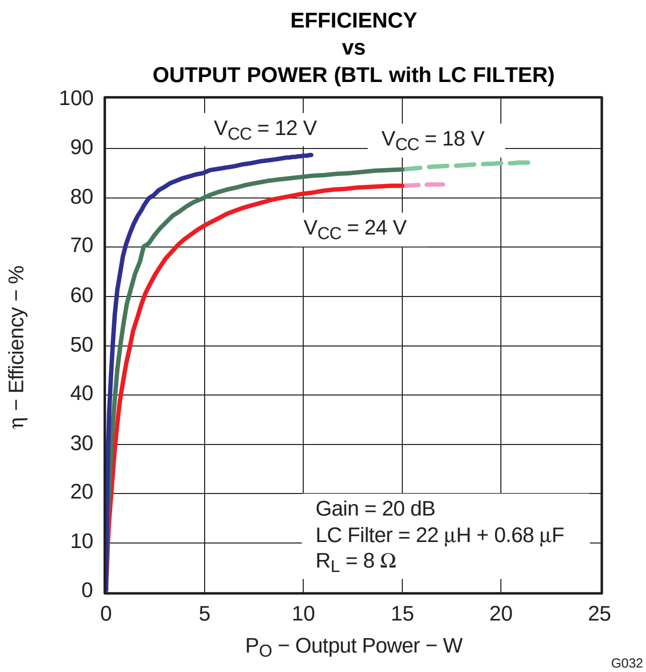
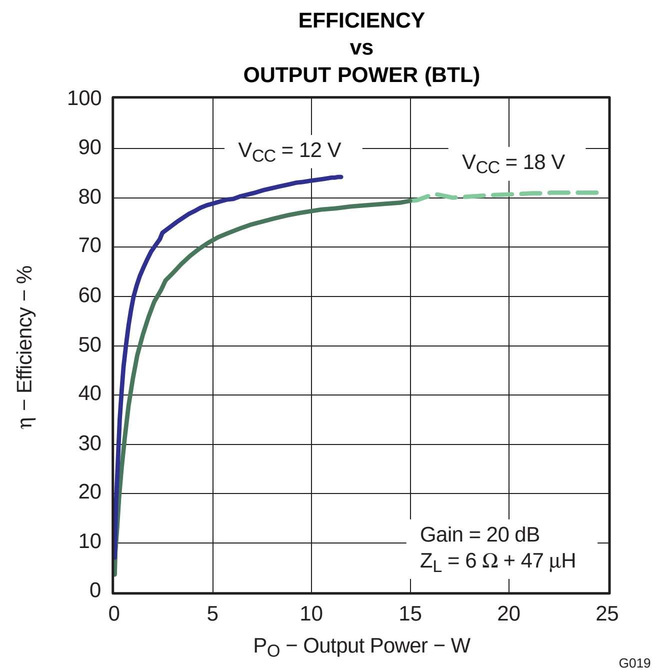


Figure 20.



Note: Dashed lines represent thermally limited regions.

Figure 21.

TYPICAL CHARACTERISTICS (continued)

All measurements taken at 1 kHz, unless otherwise noted. The TPA3110D2-Q1 EVM (which is available at ti.com) made the measurements.

EFFICIENCY vs OUTPUT POWER (BTL with LC FILTER)

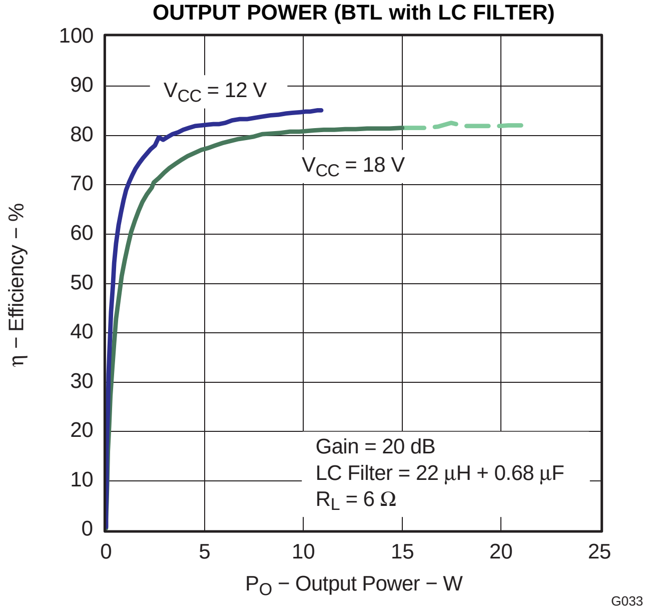


Figure 22.

EFFICIENCY vs OUTPUT POWER (BTL)

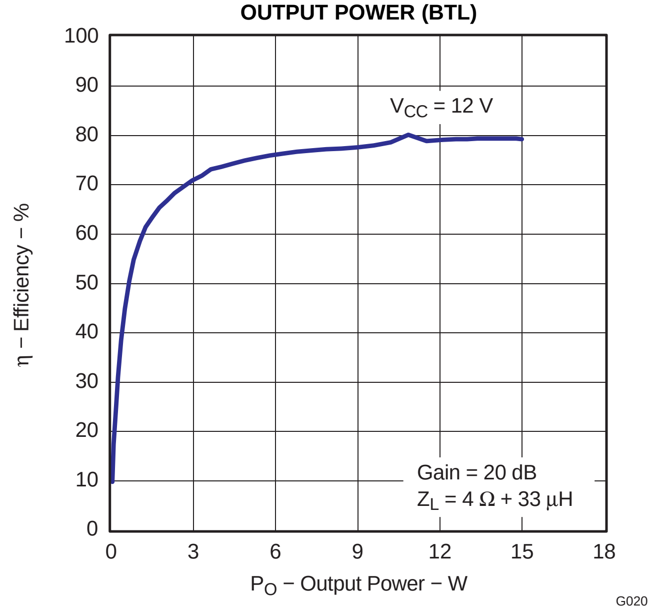


Figure 23.

EFFICIENCY vs OUTPUT POWER (BTL with LC FILTER)

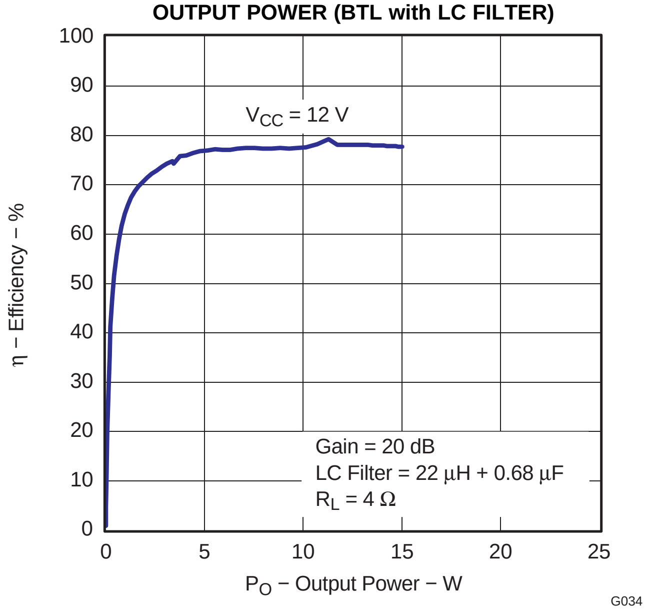
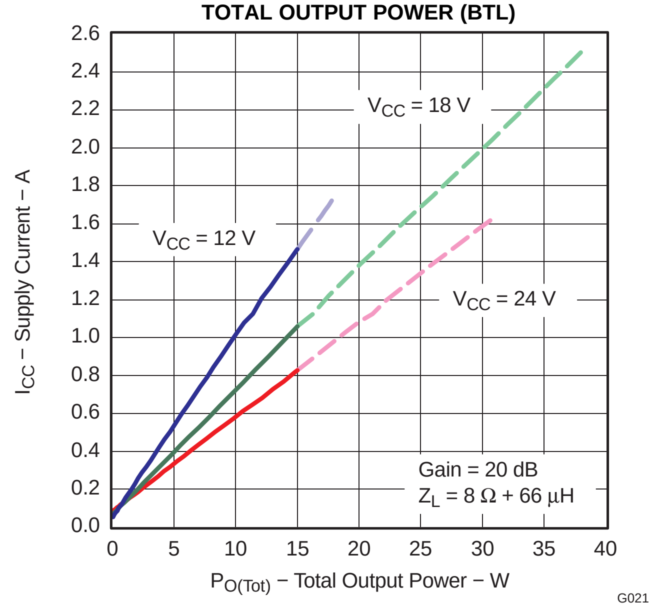


Figure 24.

SUPPLY CURRENT vs TOTAL OUTPUT POWER (BTL)

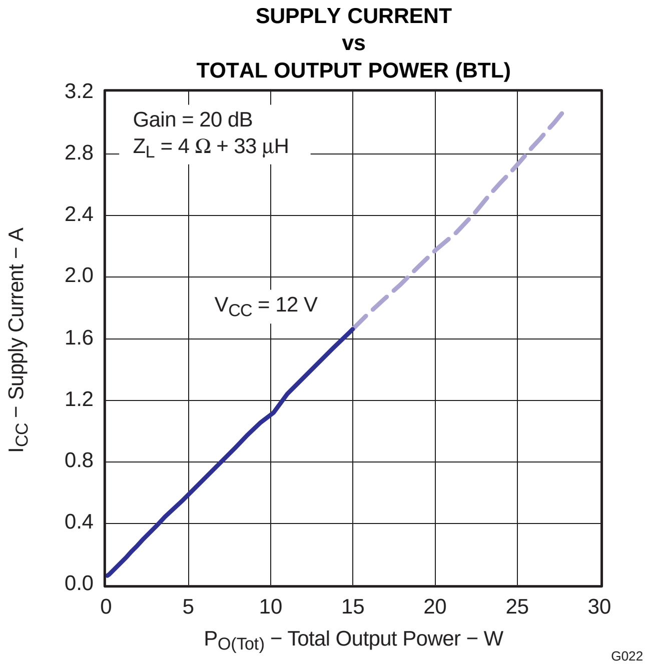


Note: Dashed lines represent thermally limited regions.

Figure 25.

TYPICAL CHARACTERISTICS (continued)

All measurements taken at 1 kHz, unless otherwise noted. The TPA3110D2-Q1 EVM (which is available at ti.com) made the measurements.



Note: Dashed lines represent thermally limited regions.

Figure 26.

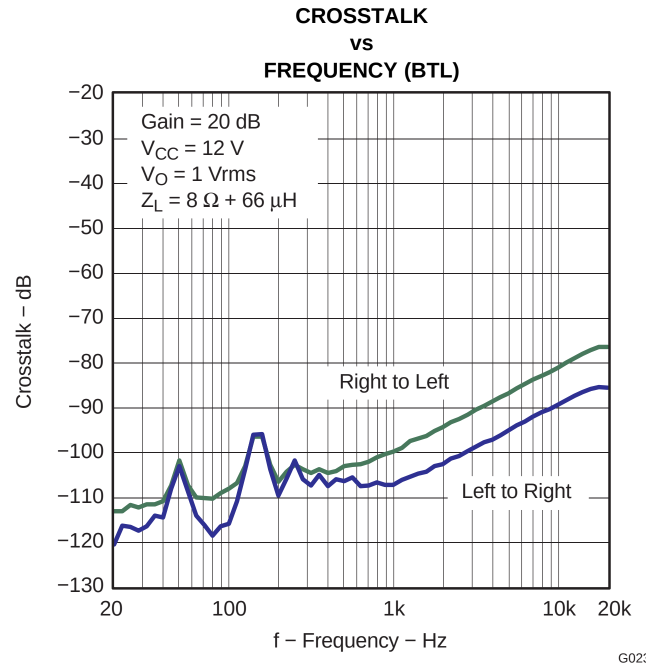


Figure 27.

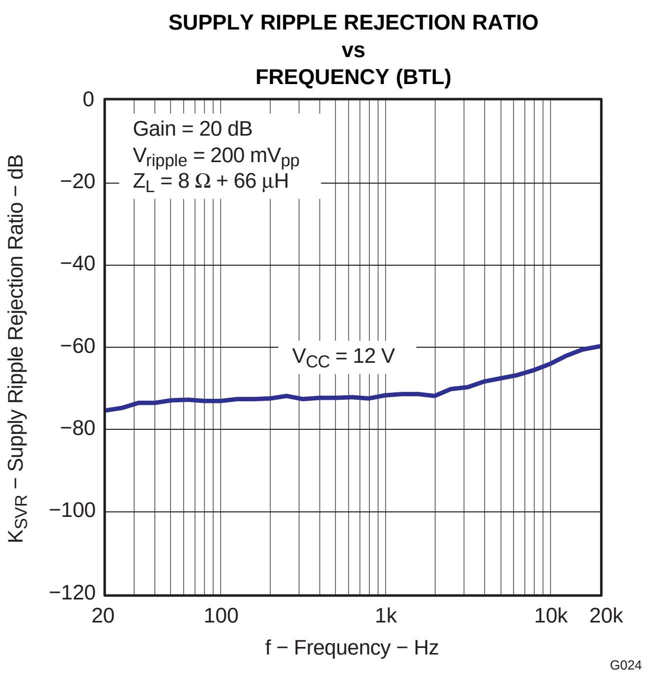


Figure 28.

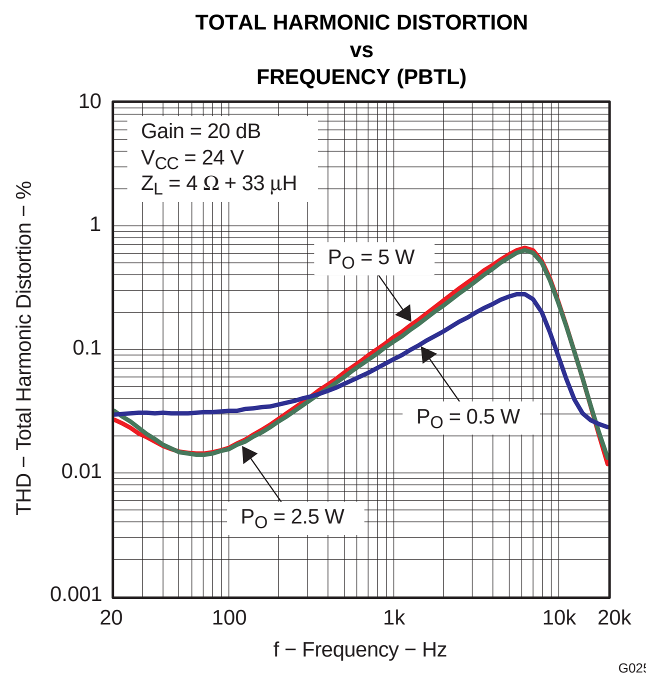


Figure 29.

TYPICAL CHARACTERISTICS (continued)

All measurements taken at 1 kHz, unless otherwise noted. The TPA3110D2-Q1 EVM (which is available at ti.com) made the measurements.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER (PBTL)

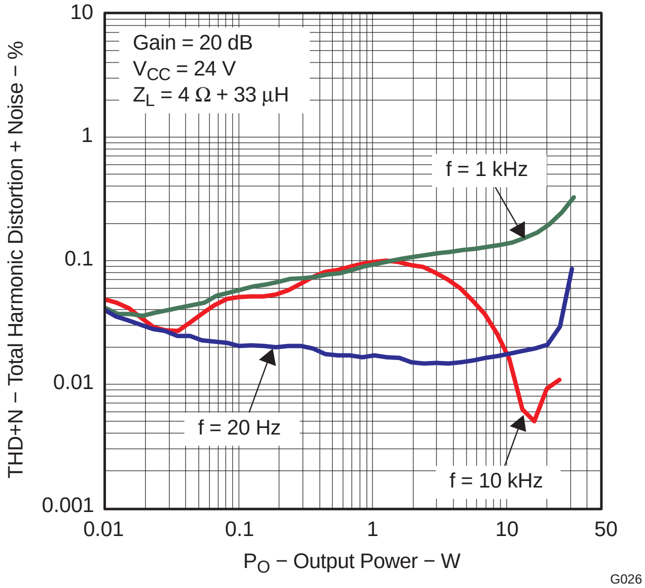


Figure 30.

GAIN/PHASE vs FREQUENCY (PBTL)

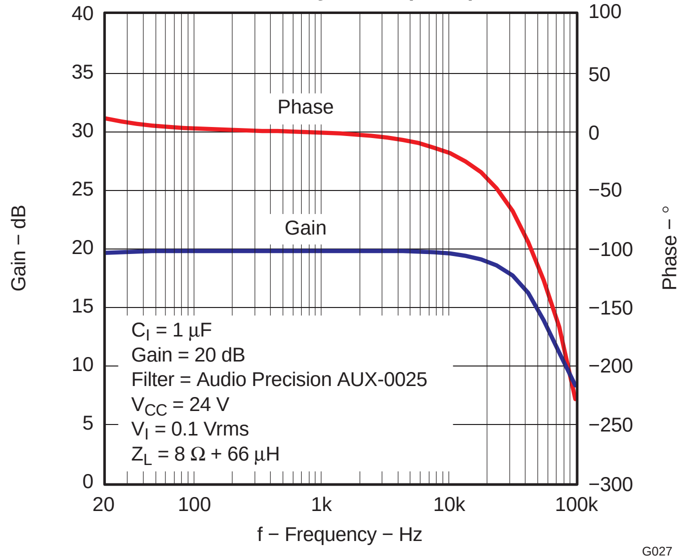
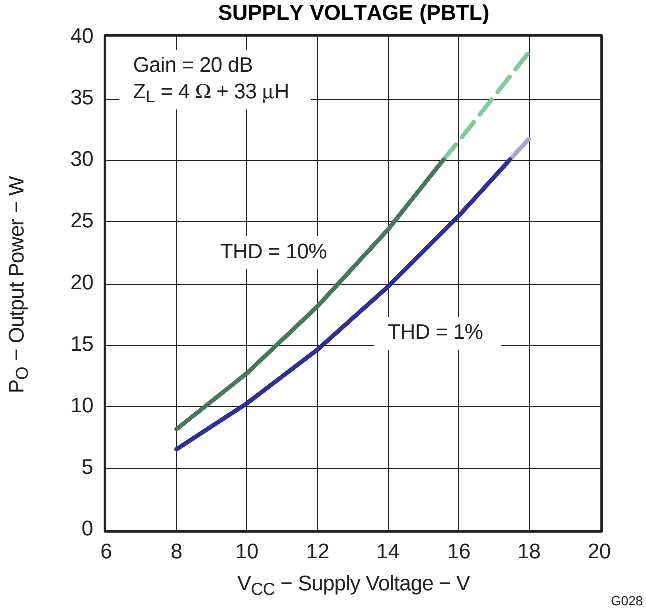


Figure 31.

OUTPUT POWER vs SUPPLY VOLTAGE (PBTL)



Note: Dashed lines represent thermally limited regions.

Figure 32.

EFFICIENCY vs OUTPUT POWER (PBTL)

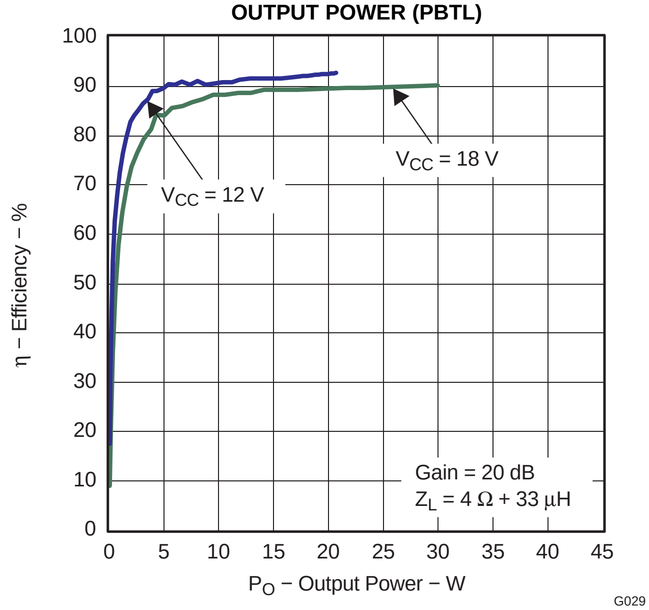


Figure 33.

TYPICAL CHARACTERISTICS (continued)

All measurements taken at 1 kHz, unless otherwise noted. The TPA3110D2-Q1 EVM (which is available at ti.com) made the measurements.

SUPPLY CURRENT vs OUTPUT POWER (PBTL)

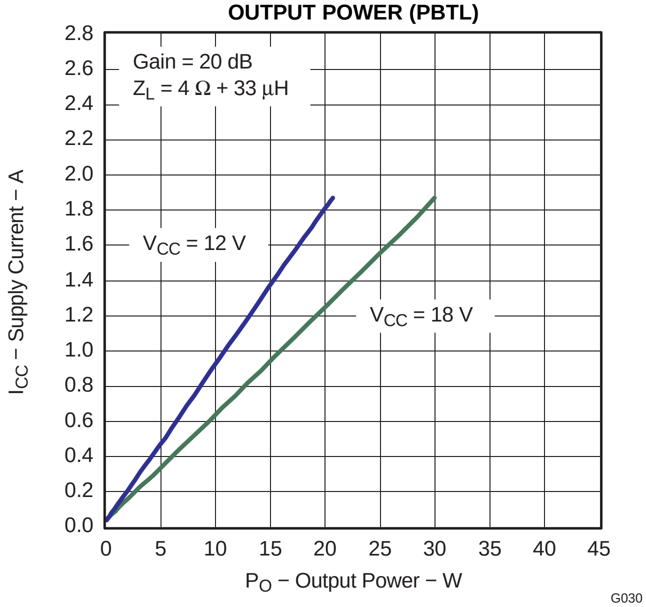


Figure 34.

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY (PBTL)

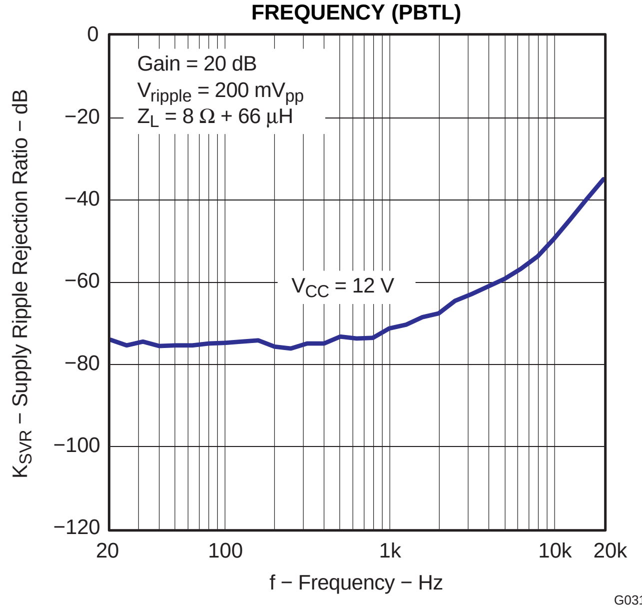


Figure 35.

DEVICE INFORMATION

Gain Setting Through GAIN0 and GAIN1 Inputs

The gain of the TPA3110D2-Q1 is set by two input terminals, GAIN0 and GAIN1. The voltage slew rate of these gain terminals, along with terminals 1 and 14, must be restricted to no more than 10 V/ms. For higher slew rates, use a 100-kΩ resistor in series with the terminals.

The gains listed in Table 1 are realized by changing the taps on the input resistors and feedback resistors inside the amplifier. This causes the input impedance (Z_I) to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the gain variation from part-to-part is small. However, the input impedance from part-to-part at the same gain may shift by ±20% due to shifts in the actual resistance of the input resistors.

For design purposes, the input network (discussed in the next section) should be designed assuming an input impedance of 7.2 kΩ, which is the absolute minimum input impedance of the TPA3110D2-Q1. At the lower gain settings, the input impedance could increase as high as 72 kΩ.

Table 1. Gain Setting

GAIN1	GAIN0	AMPLIFIER GAIN (dB)	INPUT IMPEDANCE (kΩ)
		TYP	TYP
0	0	20	60
0	1	26	30
1	0	32	15
1	1	36	9

$\overline{\text{SD}}$ OPERATION

The TPA3110D2-Q1 employs a shutdown mode of operation designed to reduce supply current (I_{CC}) to the absolute minimum level during periods of non-use for power conservation. The $\overline{\text{SD}}$ input terminal should be held high (see specification table for trip point) during normal operation when the amplifier is in use. Pulling $\overline{\text{SD}}$ low causes the outputs to mute and the amplifier to enter a low-current state. Never leave $\overline{\text{SD}}$ unconnected. When $\overline{\text{SD}}$ is not connected, amplifier operation is unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown mode prior to removing the power supply voltage.

PLIMIT

The voltage at pin 10 can be used to limit the power to levels below that which is possible based on the supply rail. Add a resistor divider from GVDD to ground to set the voltage at the PLIMIT pin. An external reference may also be used if tighter tolerance is required. Also add a 1-μF capacitor from pin 10 to ground.

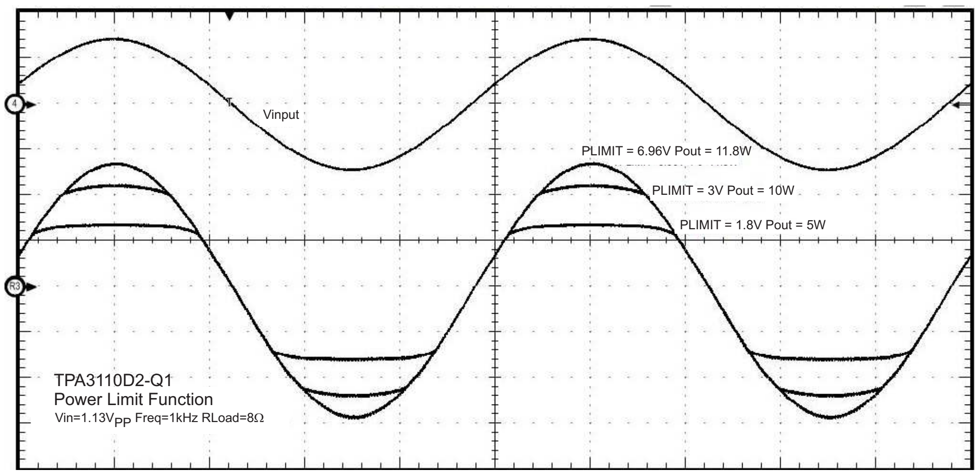


Figure 36. PLIMIT Circuit Operation

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cycle to fixed maximum value. This limit can be thought of as a virtual voltage rail which is lower than the supply connected to PVCC. This virtual rail is four times the voltage at the PLIMIT pin. This output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L} \quad \text{for unclipped power} \tag{1}$$

Where:

R_S is the total series resistance including $R_{DS(on)}$, and any resistance in the output filter.

R_L is the load resistance.

V_P is the peak amplitude of the output possible within the supply rail.

V_P = 4 × PLIMIT voltage if PLIMIT < 4 × V_P

P_{OUT} (10%THD) = 1.25 × P_{OUT} (unclipped)

Table 2. PLIMIT Typical Operation

Test Conditions ()	PLIMIT Voltage	Output Power (W)	Output Voltage Amplitude (V_{P-P})
PVCC = 24 V, V_{IN} = 1 V_{RMS}, R_L = 8 Ω, Gain = 26 dB	6.97	36.1 (thermally limited)	43
PVCC = 24 V, V_{IN} = 1 V_{RMS}, R_L = 8 Ω, Gain = 26 dB	2.94	15	25.2
PVCC = 24 V, V_{IN} = 1 V_{RMS}, R_L = 8 Ω, Gain = 26 dB	2.34	10	20
PVCC = 24 V, V_{IN} = 1 V_{RMS}, R_L = 8 Ω, Gain = 26 dB	1.62	5	14
PVCC = 24 V, V_{IN} = 1 V_{RMS}, R_L = 8 Ω, Gain = 20 dB	6.97	12.1	27.7
PVCC = 24 V, V_{IN} = 1 V_{RMS}, R_L = 8 Ω, Gain = 20 dB	3	10	23
PVCC = 24 V, V_{IN} = 1 V_{RMS}, R_L = 8 Ω, Gain = 20 dB	1.86	5	14.8
PVCC = 12 V, V_{IN} = 1 V_{RMS}, R_L = 8 Ω, Gain = 20 dB	6.97	10.55	23.5
PVCC = 12 V, V_{IN} = 1 V_{RMS}, R_L = 8 Ω, Gain = 20 dB	1.76	5	15

GVDD Supply

The GVDD supply is used to power the gates of the output full bridge transistors. It can also be used to supply the PLIMIT voltage divider circuit. Add a 1-μF capacitor to ground at this pin.

DC Detect

TPA3110D2-Q1 has circuitry which protects the speakers from DC current which might occur due to defective capacitors on the input or shorts on the printed circuit board at the inputs. A DC detect fault is reported on the $\overline{\text{FAULT}}$ pin as a low state. The DC detect fault also causes the amplifier to shut down by changing the state of the outputs to Hi-Z. To clear the DC detect it is necessary to cycle the PVCC supply. Cycling $\overline{\text{SD}}$ does NOT clear a DC detect fault.

A DC detect fault is issued when the output differential duty-cycle of either channel exceeds 14% (for example, 57%, –43%) for more than 420 msec at the same polarity. This feature protects the speaker from large DC currents or AC currents less than 2 Hz. To avoid nuisance faults due to the DC detect circuit, hold the $\overline{\text{SD}}$ pin low at power-up until the signals at the inputs are stable. Also, take care to match the impedance seen at the positive and negative inputs to avoid nuisance DC detect faults.

The minimum differential input voltages required to trigger the DC detect are shown in Table 3. The inputs must remain at or above the voltage listed in the table for more than 420 msec to trigger the DC detect.

Table 3. DC Detect Threshold

AV (dB)	V_{IN} (mV, Differential)
20	112
26	56
32	28
36	17

PBTL Select

TPA3110D2-Q1 offers the feature of parallel BTL operation with two outputs of each channel connected directly. If the PBTL pin (pin 14) is tied high, the positive and negative outputs of each channel (left and right) are synchronized and in phase. To operate in this PBTL (mono) mode, apply the input signal to the RIGHT input and place the speaker between the LEFT and RIGHT outputs. Connect the positive and negative output together for best efficiency. The voltage slew rate of the PBTL pin must be restricted to no more than 10 V/ms. For higher slew rates, use a 100-kΩ resistor in series with the terminals. For an example of the PBTL connection, see the schematic in APPLICATION INFORMATION.

For normal BTL operation, connect the PBTL pin to local ground.

SHORT-CIRCUIT PROTECTION AND AUTOMATIC RECOVERY FEATURE

TPA3110D2-Q1 has protection from overcurrent conditions caused by a short circuit on the output stage. The short-circuit protection fault is reported on the $\overline{\text{FAULT}}$ pin as a low state. The amplifier outputs are switched to a Hi-Z state when the short-circuit protection latch is engaged. The latch can be cleared by cycling the $\overline{\text{SD}}$ pin through the low state.

If automatic recovery from the short-circuit protection latch is desired, connect the $\overline{\text{FAULT}}$ pin directly to the $\overline{\text{SD}}$ pin. This allows the $\overline{\text{FAULT}}$ pin function to automatically drive the $\overline{\text{SD}}$ pin low, which clears the short-circuit protection latch.

THERMAL PROTECTION

Thermal protection on the TPA3110D2-Q1 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 15°C. The device begins normal operation at this point with no external system interaction.

Thermal protection faults are NOT reported on the $\overline{\text{FAULT}}$ terminal.

APPLICATION INFORMATION

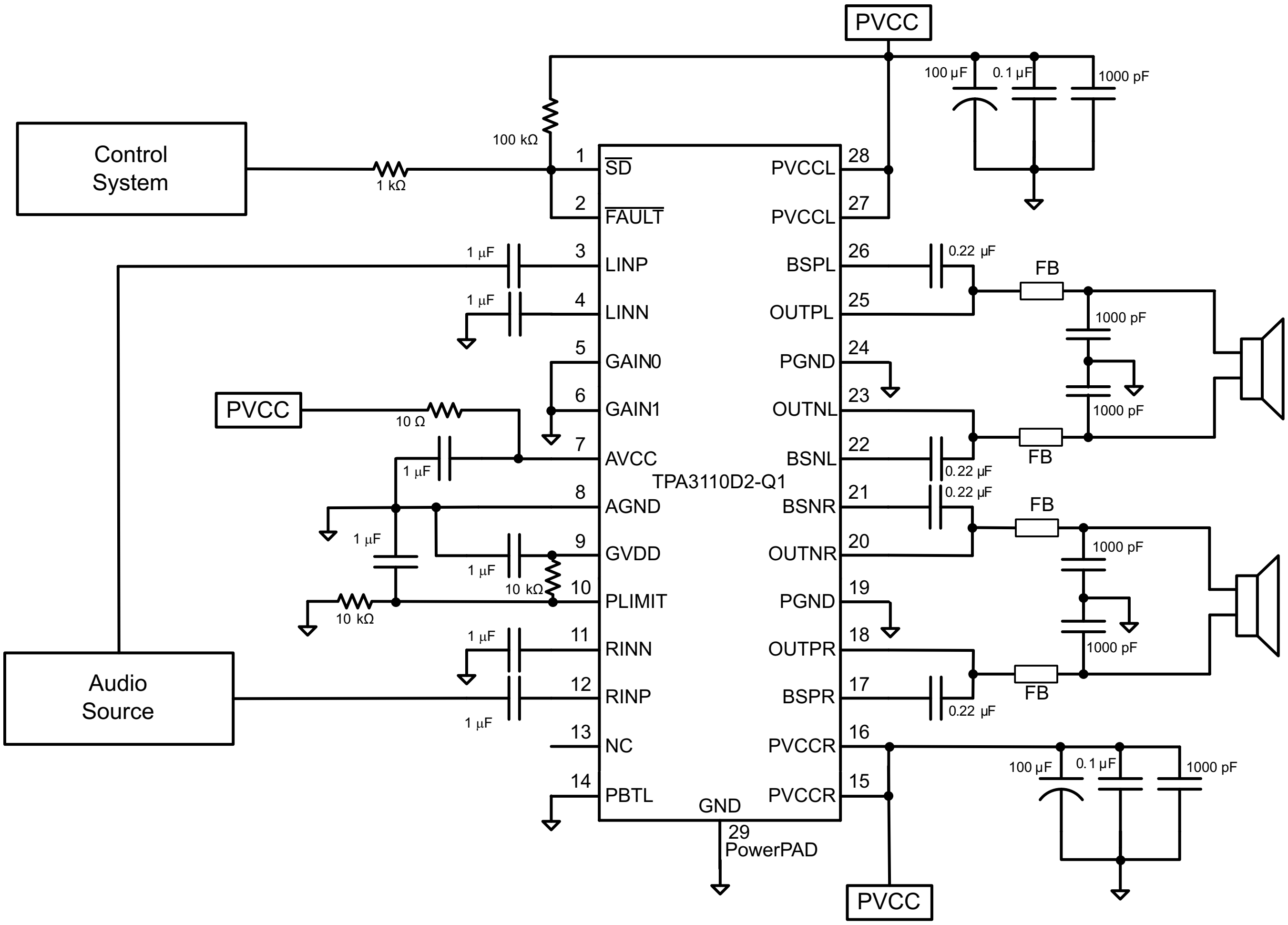
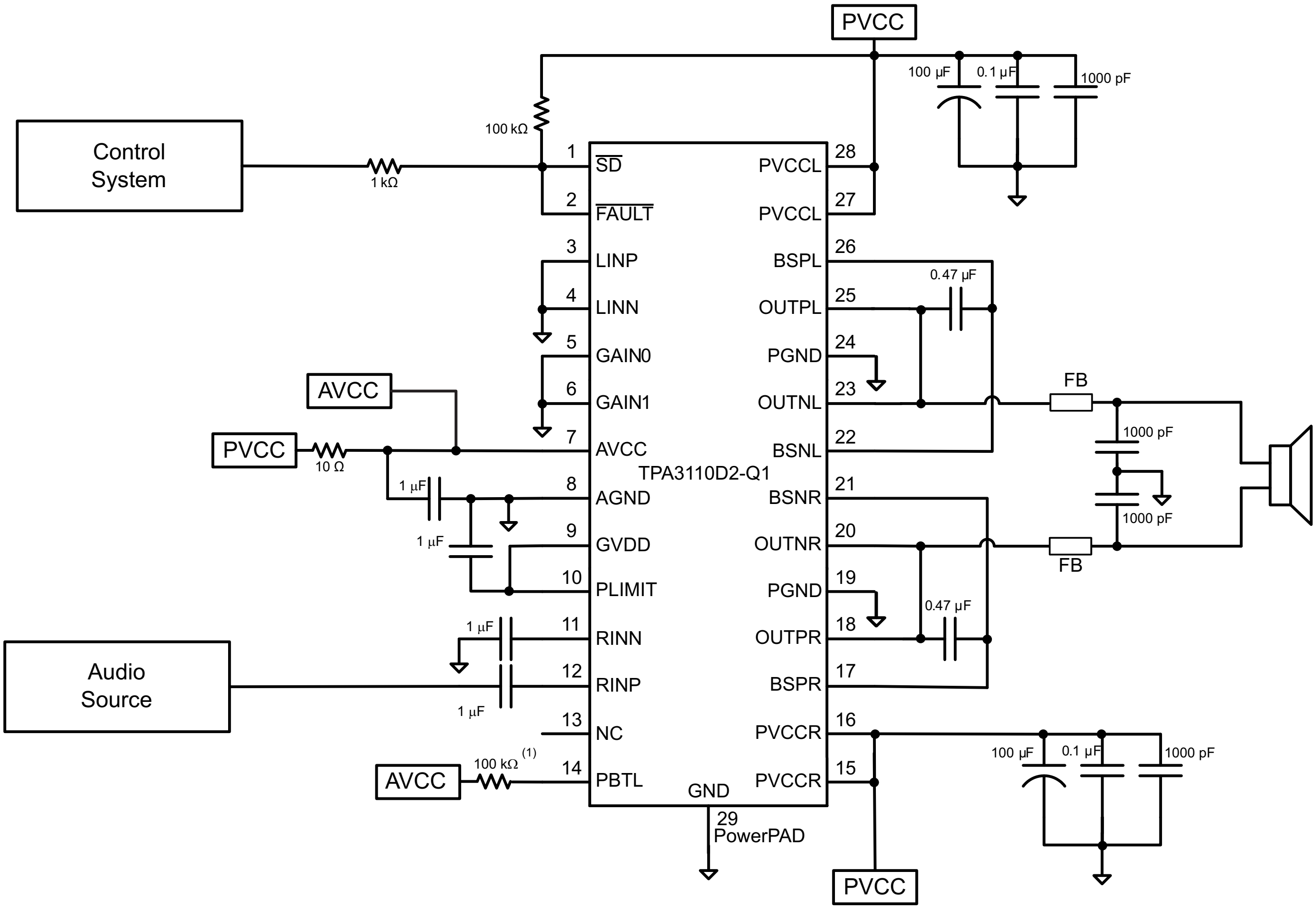


Figure 37. Stereo Class-D Amplifier with BTL Output and Single-Ended Inputs with Power Limiting



(1) A 100-kΩ resistor is needed if the PVCC slew rate is more than 10 V/ms.

Figure 38. Stereo Class-D Amplifier With PBTL Output and Single-Ended Input

TPA3110D2-Q1 Modulation Scheme

The TPA3110D2-Q1 uses a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load. Each output is switching from 0 volts to the supply voltage. The OUTP and OUTN are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTP is greater than 50% and OUTN is less than 50% for positive output voltages. The duty cycle of OUTP is less than 50% and OUTN is greater than 50% for negative output voltages. The voltage across the load sits at 0 V throughout most of the switching period, reducing the switching current, which reduces any I^2R losses in the load.

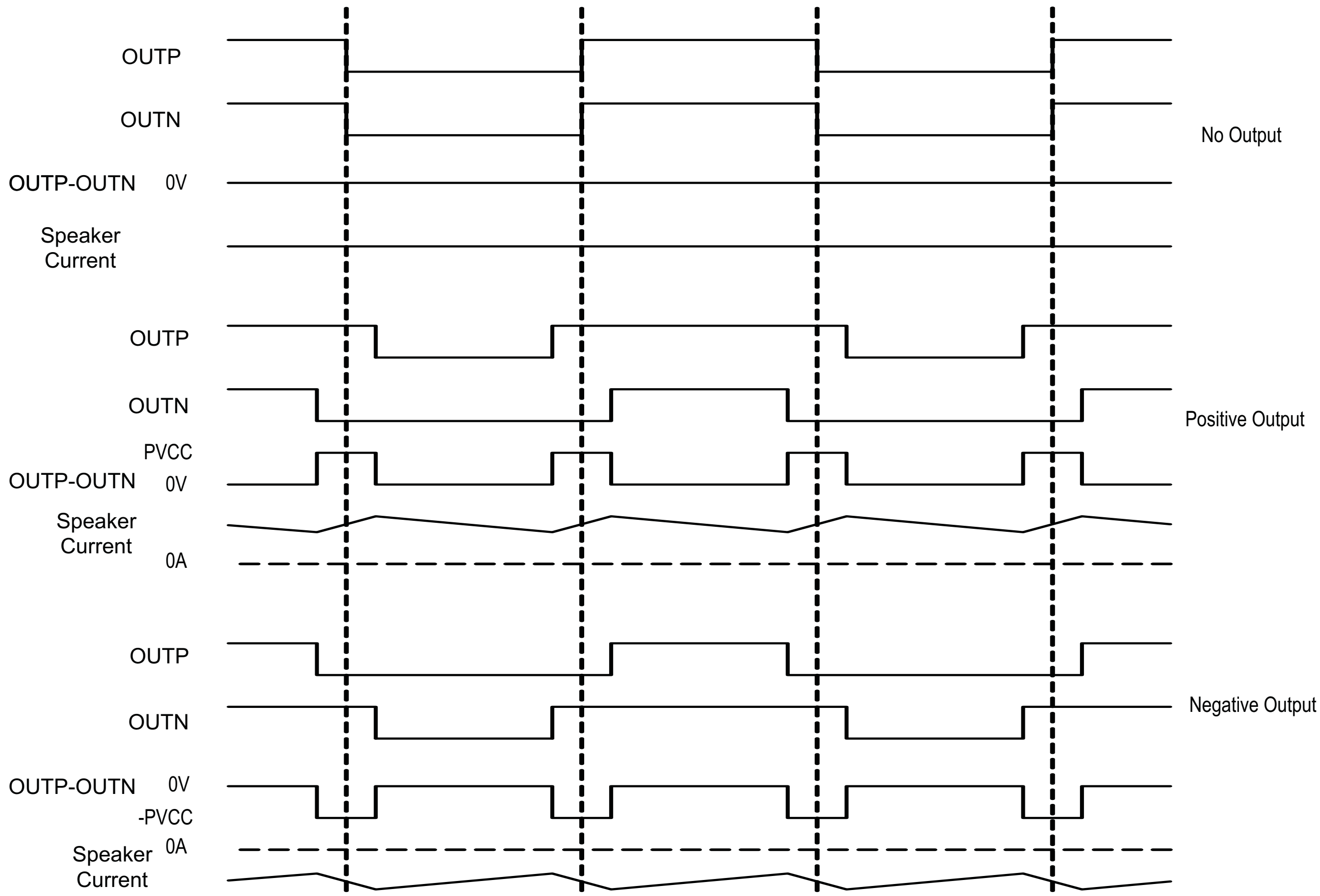


Figure 39. The TPA3110D2-Q1 Output Voltage and Current Waveforms Into an Inductive Load

Ferrite Bead Filter Considerations

Using the advanced emissions suppression technology in the TPA3110D2-Q1 amplifier, it is possible to design a high efficiency Class-D audio amplifier while minimizing interference to surrounding circuits. It is also possible to accomplish this with only a low-cost ferrite bead filter. In this case it is necessary to carefully select the ferrite bead used in the filter.

One important aspect of the ferrite bead selection is the type of material used in the ferrite bead. Not all ferrite material is alike, so it is important to select a material that is effective in the 10- to 100-MHz range which is key to the operation of the Class-D amplifier. Many of the specifications regulating consumer electronics have emissions limits as low as 30 MHz. It is important to use the ferrite bead filter to block radiation in the 30-MHz and above range from appearing on the speaker wires and the power supply lines which are good antennas for these signals. The impedance of the ferrite bead can be used along with a small capacitor with a value in the range of 1000 pF to reduce the frequency spectrum of the signal to an acceptable level. For best performance, the resonant frequency of the ferrite bead and capacitor filter should be less than 10 MHz.

Also, it is important that the ferrite bead is large enough to maintain its impedance at the peak currents expected for the amplifier. Some ferrite bead manufacturers specify the bead impedance at a variety of current levels. In this case it is possible to make sure the ferrite bead maintains an adequate amount of impedance at the peak current the amplifier sees. If these specifications are not available, it is also possible to estimate the bead current handling capability by measuring the resonant frequency of the filter output at low power and at maximum power. A change of resonant frequency of less than fifty percent under this condition is desirable. Examples of tested ferrite beads that work well with the TPA3110D2-Q1 include 28L0138-80R-10 and HI1812V101R-10 from Steward and the 742792510 from Wurth Electronics.

A high quality ceramic capacitor is also needed for the ferrite bead filter. A low ESR capacitor with good temperature and voltage characteristics works best.

Additional EMC improvements may be obtained by adding snubber networks from each of the Class-D outputs to ground. Suggested values for a simple RC series snubber network would be 10 Ω in series with a 330-pF capacitor although design of the snubber network is specific to every application and must be designed taking into account the parasitic reactance of the printed circuit board as well as the audio amp. Take care to evaluate the stress on the component in the snubber network especially if the amp is running at high PVCC. Also, make sure the layout of the snubber network is tight and returns directly to the PGND or the PowerPAD™ integrated circuit package beneath the chip.

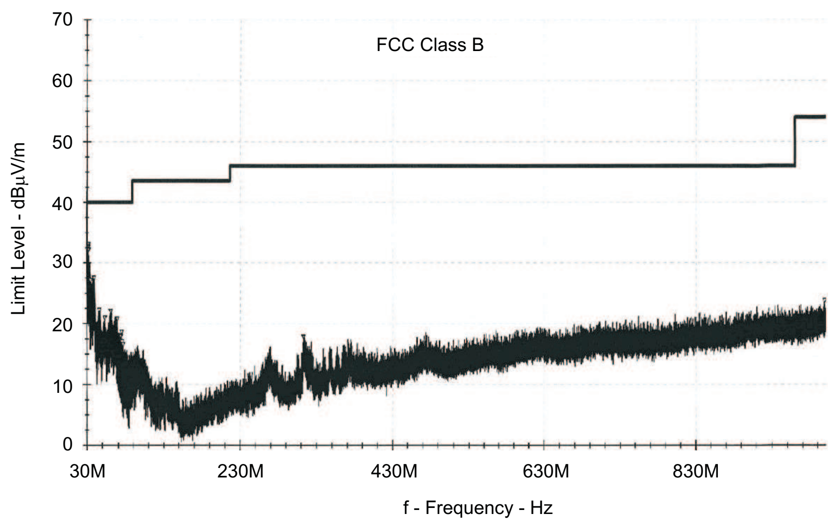


Figure 40. TPA3110D2-Q1 EMC Spectrum With FCC Class-B Limits

Efficiency: LC Filter Required With the Traditional Class-D Modulation Scheme

The main reason that the traditional Class-D amplifier needs an output filter is because the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is $2 \times V_{CC}$, and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The TPA3110D2-Q1 modulation scheme has little loss in the load without a filter because the pulses are short and the change in voltage is V_{CC} instead of $2 \times V_{CC}$. As the output power increases, the pulses widen, making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cutoff frequency less than the Class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance but higher impedance at the switching frequency than the speaker, which results in less power dissipation, therefore increasing efficiency.

When to Use an Output Filter for EMI Suppression

The TPA3110D2-Q1 has been tested with a simple ferrite bead filter for a variety of applications including long speaker wires up to 125 cm and high power. The TPA3110D2-Q1 EVM passes FCC Class-B specifications under these conditions using twisted speaker wires. The size and type of ferrite bead can be selected to meet application requirements. Also, the filter capacitor can be increased if necessary with some impact on efficiency.

There may be a few circuit instances where it is necessary to add a complete LC reconstruction filter. These circumstances might occur if there are nearby circuits which are sensitive to noise. In these cases a classic second order Butterworth filter similar to those shown in the figures below can be used.

Some systems have little power supply decoupling from the AC line but are also subject to line conducted interference (LCI) regulations. These include systems powered by wall warts and power bricks. In these cases, the LC reconstruction filters can be the lowest cost means to pass LCI tests. Common mode chokes using low frequency ferrite material can also be effective at preventing line conducted interference.

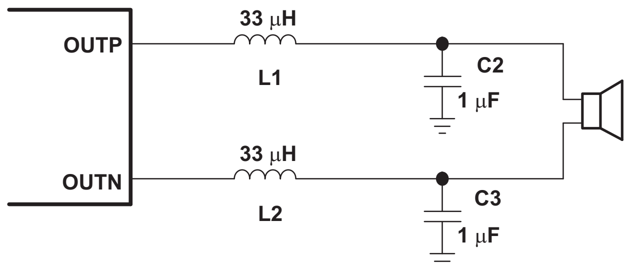


Figure 41. Typical LC Output Filter, Cutoff Frequency of 27 kHz, Speaker Impedance = 8 Ω

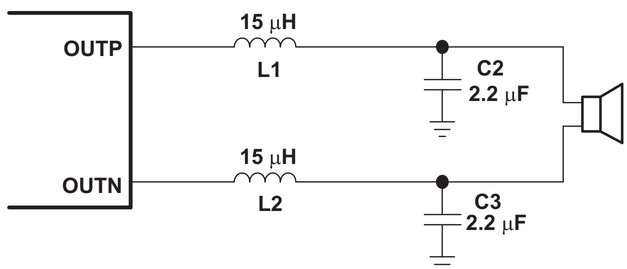


Figure 42. Typical LC Output Filter, Cutoff Frequency of 27 kHz, Speaker Impedance = 4 Ω

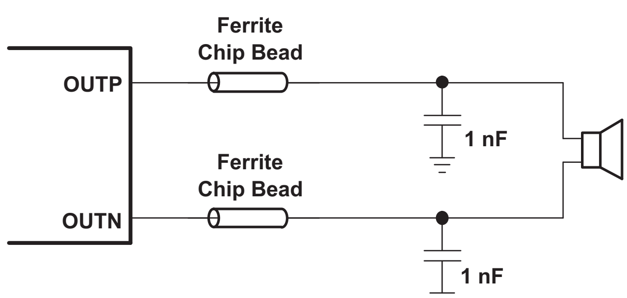
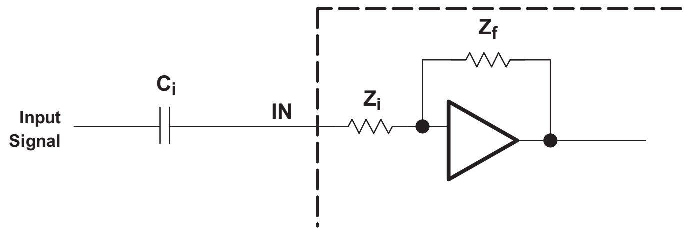


Figure 43. Typical Ferrite Chip Bead Filter (Chip Bead Example)

INPUT RESISTANCE

Changing the gain setting can vary the input resistance of the amplifier from its smallest value, 9 kΩ ±20%, to the largest value, 60 kΩ ±20%. As a result, if a single capacitor is used in the input high-pass filter, the –3 dB or cutoff frequency may change when changing gain steps.



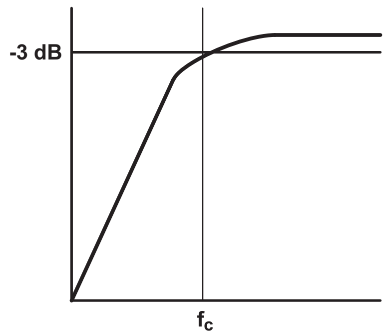
The –3-dB frequency can be calculated using Equation 2. Use the Z_I values given in Table 1.

$$f = \frac{1}{2\pi Z_i C_i} \tag{2}$$

INPUT CAPACITOR, C_I

In the typical application, an input capacitor (C_I) is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C_I and the input impedance of the amplifier (Z_I) form a high-pass filter with the corner frequency determined in Equation 3.

$$f_c = \frac{1}{2\pi Z_i C_i} \tag{3}$$



The value of C_I is important, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where Z_I is 60 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 3 is reconfigured as Equation 4.

$$C_i = \frac{1}{2\pi Z_i f_c} \tag{4}$$

In this example, C_I is 0.13 µF; so, one would likely choose a value of 0.15 μF as this value is commonly used. If the gain is known and is constant, use Z_I from Table 1 to calculate C_I. A further consideration for this capacitor is the leakage path from the input source through the input network (C_I) and the feedback network to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the DC level there is held at 3 V, which is likely higher than the source DC level. Note that it is important to confirm the capacitor polarity in the application. Additionally, lead-free solder can create DC offset voltages and it is important to ensure that boards are cleaned properly.

POWER SUPPLY DECOUPLING, C_S

The TPA3110D2-Q1 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. Optimum decoupling is achieved by using a network of capacitors of different types that target specific types of noise on the power supply leads. For higher frequency transients due to parasitic circuit elements such as bond wire and copper trace inductances as well as lead frame capacitance, a good quality low equivalent-series-resistance (ESR) ceramic capacitor of value between 220 pF and 1000 pF works well. This capacitor should be placed as close to the device PVCC pins and system ground (either PGND pins or PowerPAD™ integrated circuit package) as possible. For mid-frequency noise due to filter resonances or PWM switching transients as well as digital hash on the line, another good quality capacitor typically 0.1 µF to 1 µF placed as close as possible to the device PVCC leads works best. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 220 µF or greater placed near the audio power amplifier is recommended. The 220-µF capacitor also serves as a local storage capacitor for supplying current during large signal transients on the amplifier outputs. The PVCC terminals provide the power to the output transistors, so a 220-µF or larger capacitor should be placed on each PVCC terminal. A 10-µF capacitor on the AVCC terminal is adequate. Also, a small decoupling resistor between AVCC and PVCC can be used to keep high frequency Class-D noise from entering the linear input amplifiers.

BSN and BSP CAPACITORS

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 0.22-µF ceramic capacitor, rated for at least 25 V, must be connected from each output to its corresponding bootstrap input. Specifically, one 0.22-µF capacitor must be connected from OUTPx to BSPx, and one 0.22-µF capacitor must be connected from OUTNx to BSNx. (See the application circuit diagram in Figure 1.)

The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

DIFFERENTIAL INPUTS

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the TPA3110D2-Q1 with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the TPA3110D2-Q1 with a single-ended source, AC-ground the INP or INN input through a capacitor equal in value to the input capacitor on INN or INP and apply the audio source to either input. In a single-ended input application, the unused input should be AC-grounded at the audio source instead of at the device input for best noise performance. For good transient performance, the impedance seen at each of the two differential inputs should be the same.

The impedance seen at the inputs should be limited to an RC time constant of 1 ms or less if possible. This is to allow the input DC blocking capacitors to become completely charged during the 14 ms power-up time. If the input capacitors are not allowed to completely charge, there will be some additional sensitivity to component matching which can result in pop if the input components are not well matched.

USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

PRINTED-CIRCUIT BOARD (PCB) LAYOUT

The TPA3110D2-Q1 can be used with a small, inexpensive ferrite bead output filter for most applications. However, since the Class-D switching edges are fast, it is necessary to take care when planning the layout of the printed circuit board. The following suggestions help to meet EMC requirements.

- Decoupling capacitors—The high-frequency decoupling capacitors should be placed as close to the PVCC and AVCC terminals as possible. Large (220-µF or greater) bulk power supply decoupling capacitors should be placed near the TPA3110D2-Q1 on the PVCCL and PVCCR supplies. Local, high-frequency bypass capacitors should be placed as close to the PVCC pins as possible. These caps can be connected to the thermal pad directly for an excellent ground connection. Consider adding a small, good quality low ESR ceramic capacitor between 220 pF and 1000 pF and a larger good quality mid-frequency cap of value between 0.1 µF and 1 µF to the PVCC connections at each end of the chip.
- Keep the current loop from each of the outputs through the ferrite bead and the small filter cap and back to PGND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.
- Grounding—The AVCC (pin 7) decoupling capacitor should be grounded to analog ground (AGND). The PVCC decoupling capacitors should connect to PGND. Analog ground and power ground should be connected at the thermal pad, which should be used as a central ground connection or star ground for the TPA3110D2-Q1.
- Output filter—The ferrite EMI filter (Figure 43) should be placed as close to the output terminals as possible for the best EMI performance. The LC filter (Figure 41 and Figure 42) should be placed close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded to power ground.
- Thermal pad—The thermal pad must be soldered to the PCB for proper thermal performance and optimal reliability. The dimensions of the thermal pad and thermal land should be 6.46 mm by 2.35 mm. Seven rows of solid vias (three vias per row, 0,3302 mm or 13 mils diameter) should be equally spaced underneath the thermal land. The vias should connect to a solid copper plane, either on an internal layer or on the bottom layer of the PCB. The vias must be solid vias, not thermal relief or webbed vias. See the TI Application Report SLMA002 for more information about using the TSSOP thermal pad. For recommended PCB footprints, see the figures at the end of this data sheet.

For an example layout, see the TPA3110D2-Q1 Evaluation Module (TPA3110D2-Q1 EVM) User's Guide. Both the EVM user's guide and the thermal pad application report are available on the TI website at http://www.ti.com.

REVISION HISTORY

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPA3110D2QPWPRQ1	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF TPA3110D2-Q1 :

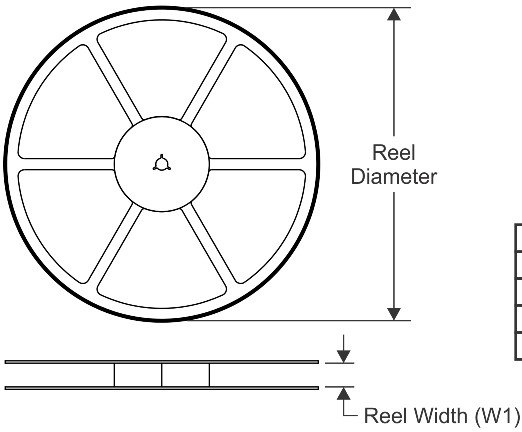
- Catalog: TPA3110D2

NOTE: Qualified Version Definitions:

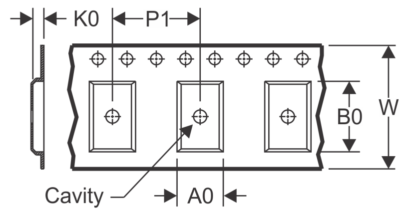
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

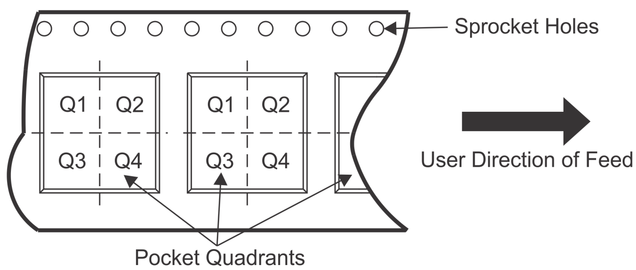


TAPE DIMENSIONS



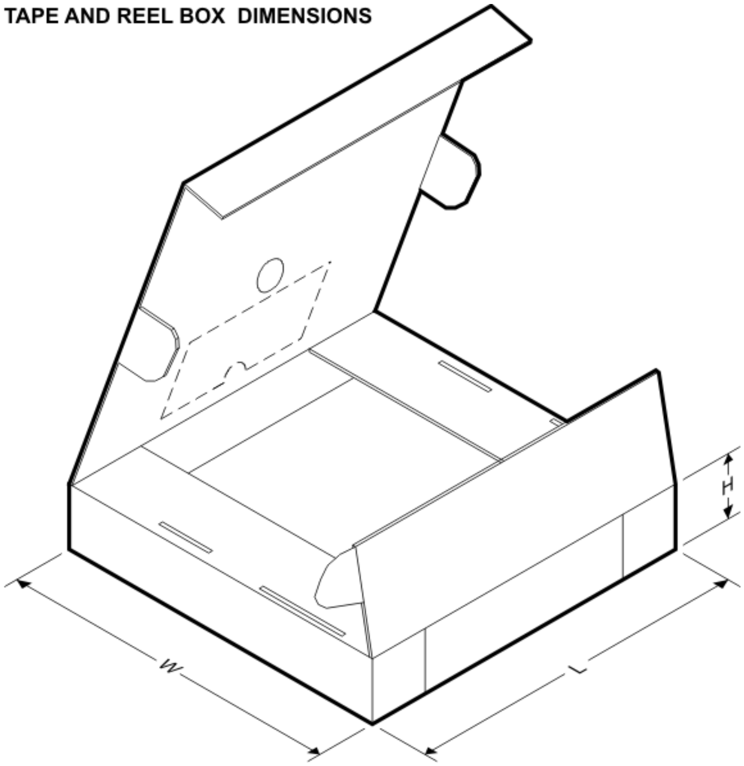
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

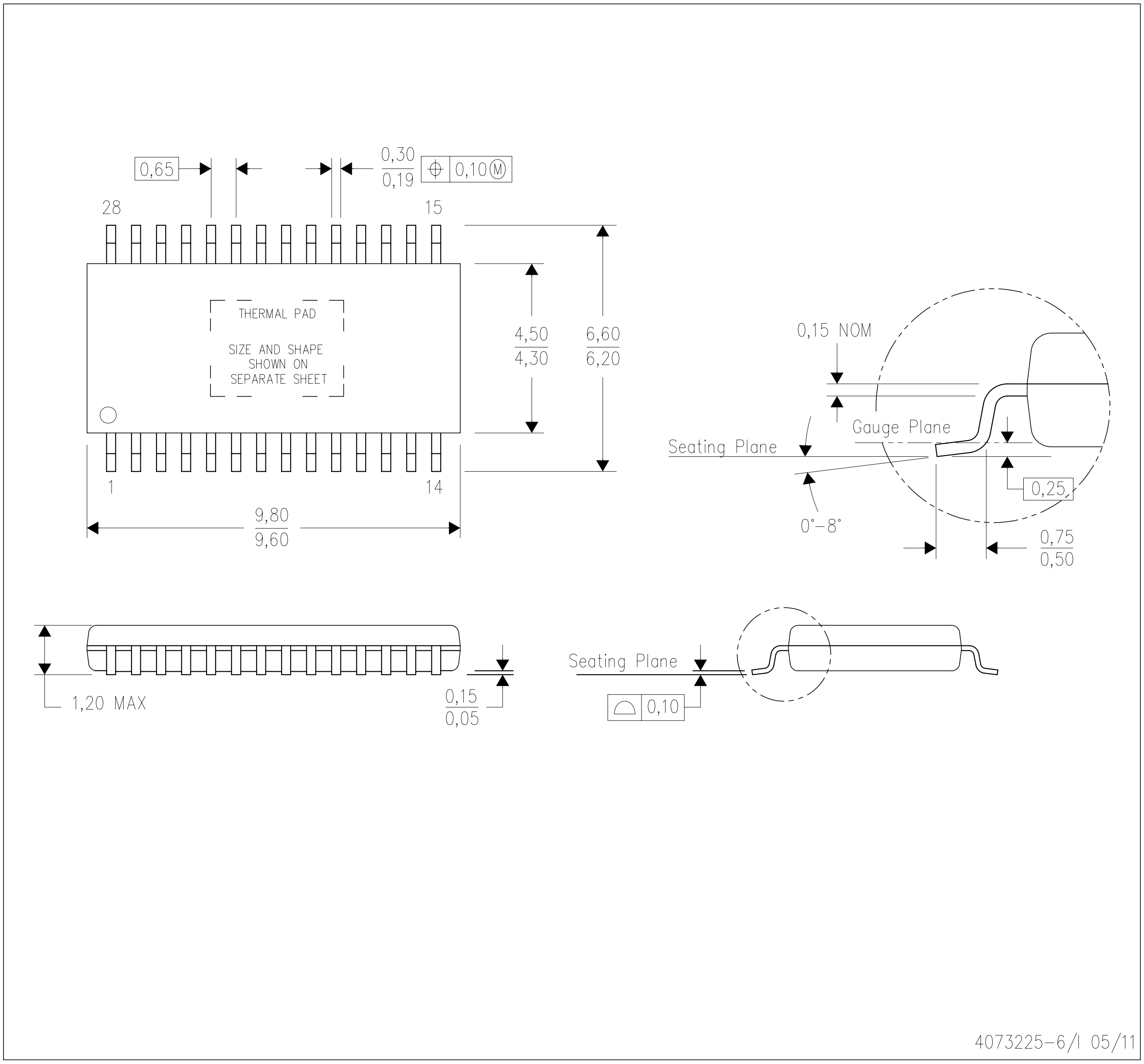
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA3110D2QPWPRQ1	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA3110D2QPWPRQ1	HTSSOP	PWP	28	2000	367.0	367.0	38.0

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

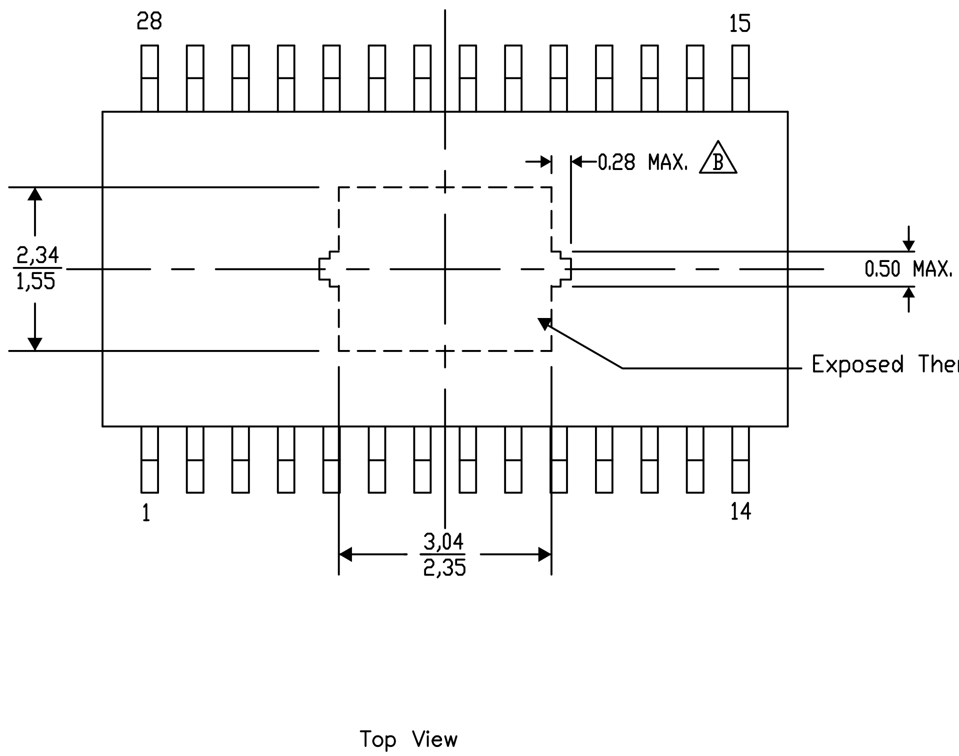
PWP (R-PDSO-G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

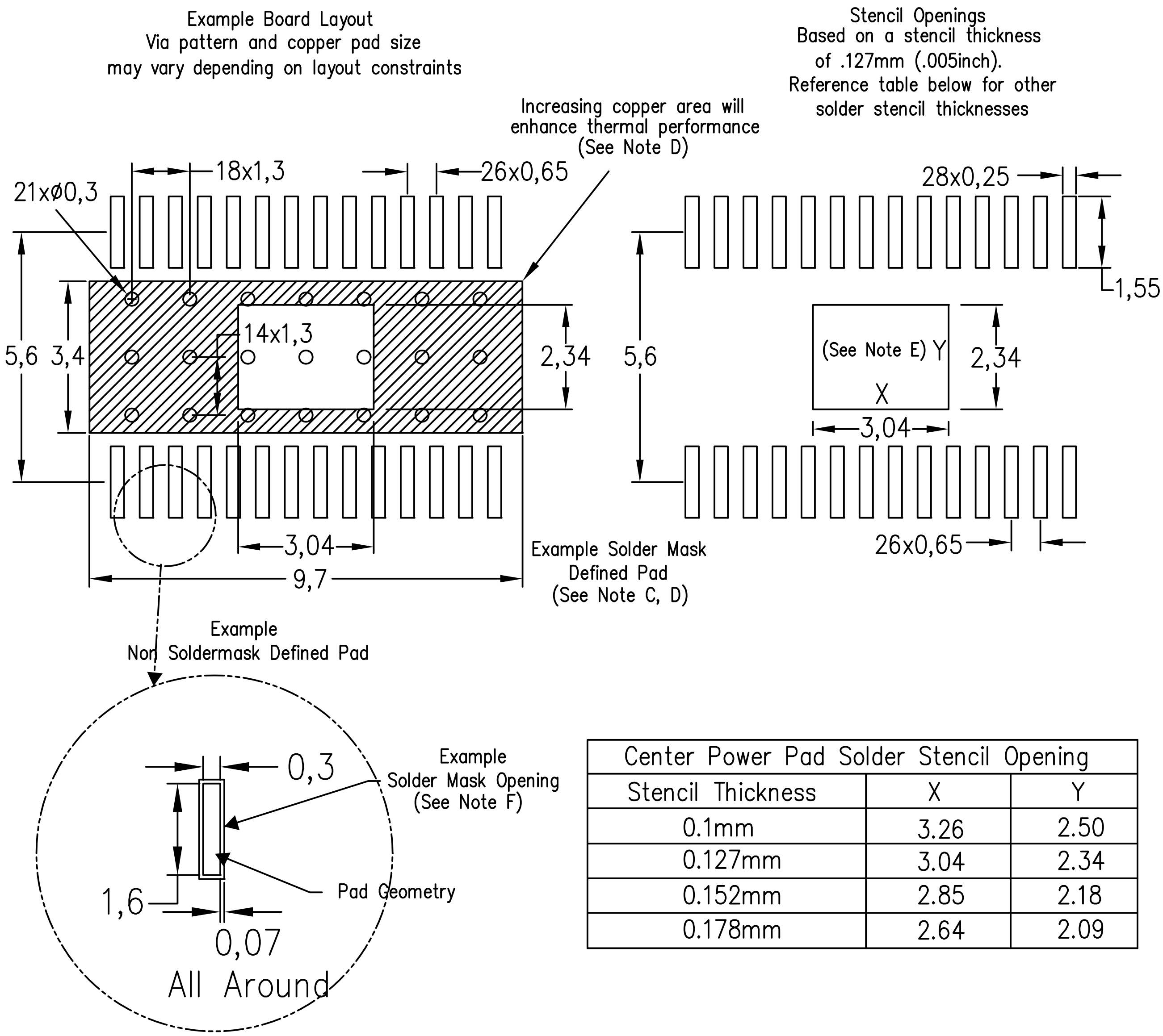
4206332-39/AC 07/12

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G28) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.26	2.50
0.127mm	3.04	2.34
0.152mm	2.85	2.18
0.178mm	2.64	2.09

4207609-23/R 07/12

NOTES:

A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.

D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>. Publication IPC-7351 is recommended for alternate designs.

E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265