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PMIC for LCD TV / Monitor

General Description

The CM501 generates all the supply rails for thin-film transistor (TFT) liquid-crystal display (LCD) panels in TVs and Monitors. It includes boost and buck regulators, VGH and VGL charge pump regulators, gate pulse modulator (GPM) , HV LDO, voltage detector (XAO) and VCOM OP. The CM501 can support input voltage from 8V to 14V and is optimized for LCD TV panel and LCD monitor applications running directly from 12V supply.

The boost and buck regulators feature internal power MOSFETs and high-frequency operation allowing the use of small inductors and capacitors, resulting in a compact solution. Both switching regulators use fixed-frequency, current-mode control architectures, providing fast load-transient response and easy compensation.

The VGH and VGL charge-pump regulators provide supply voltages for TFT gate driver. Both output voltages can be adjusted with external resistive voltage dividers.

The GPM is controlled by frame signals from timing controller to modulate the Gate-On voltage (VGHM), which acts as a flicker compensation to reduce the coupling effect between gate lines and pixels. It also can delay VGHM while power-on for achieving a correct power-on sequence for gate driver ICs. VGHM power-on delay time, the falling time and falling stop voltage can be programmable by an external capacitor and an external resistor.

The voltage detector (XAO) monitors VIN voltage to issue a reset signal while the detected voltage is too low. The detecting level is decided by an external resistive voltage divider.

The HV LDO can provide a highly accurate voltage (0.5%) for gamma reference voltage. It has fast transient response and also wide operation input range.

The VCOM OP can drive the LCD VCOM voltage that features high short-circuit current (300mA), fast slew rate (45V/μs), wide bandwidth (20MHz) and rail-to-rail inputs and outputs.

The CM501 is available in a small WQFN-48L 7x7 package and operates over the -40°C to +85°C temperature range.

Features

- **8V to 14V Supply Input Voltage Range**
- **Current-Mode Boost Regulator**
  - **20V 3.5A 0.1Ω Internal N-MOSFET**
  - **Programmable Over Current Protection Voltage**
  - **±1% Accurate Output**
  - **Progremmable Soft-start**
  - **Line Regulation 0.15%/V**
  - **Load Regulation ±1%/A**
  - **External Compensation**
- **Current-Mode Buck Regulator**
  - **16.5V 3.2A 0.15Ω Internal N-MOSFET**
  - **Over Current Protection**
  - **Adjustable Output Voltage from 1.8V to 3.3V**
  - **±1% Accurate Output**
  - **Line Regulation 0.1%/V**
  - **Load Regulation ±0.5%/A**
  - **Internal Compensation**
  - **Internal Soft-start**
- **Adjustable VGH Charge Pump**
  - **±2% Accurate Output**
  - **Continuous Output Current 50mA**
- **Adjustable VGL Charge Pump**
  - **Accurate Output Controlled by (REF– FBN)**
  - **Continuous Output Current 50mA**
- **Gate Pulse Modulator**
  - **18V to 35V Positive Supply Input**
  - **Flicker Compensation**
  - **Power-On/Off Sequence Control**
  - **On-Chip GPM Controller with Adjustable Falling Time and Falling Stop Voltage**
- **Voltage Detector (XAO)**
  - **Adjustable Detecting Voltage (±1%)**
  - **N-Channel Open-Drain Output**
- **VCOM OP**
  - **5V to 20V Input Supply Voltage**
  - **±300mA Output Short-Circuit Current for 1ms**
  - **45V/μs Slew Rate**
  - **20MHz, –3dB Bandwidth**
  - **Rail-to-Rail Input/Output**

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- **HV LDO**
- **5V to 20V Input Supply Voltage**
- **Adjustable Output Voltage (±0.5%)**
- **Over Current Protection (60mA)**
- **Low Dropout Voltage 0.5V (60mA)**
- **Selectable Frequency (500kHz/750KHz)**
- **External PMOS Isolation Switch Controlled by Gate Drive Signal**
- **Under Voltage Protection**
- **Short Circuit Protection**
- **Over Temperature Protection**
- **Power On Sequence Control**
- **Thin 48-Lead WQFN Package**

Applications

- LCD TV / Monitor

Marking Information

CM501 : Product Number

YMDNN : Date Code

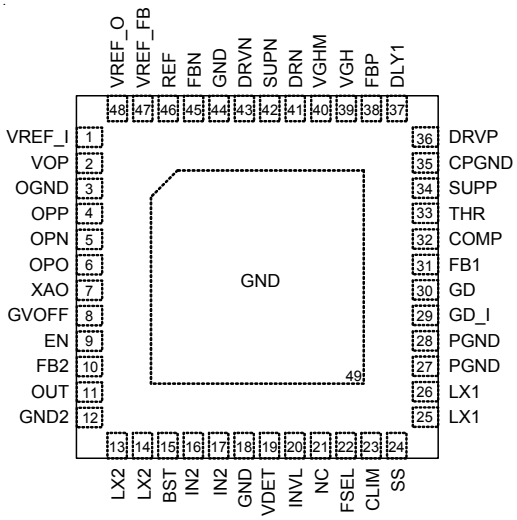
R1 : Richteck

01 : Revision

YYWW : Week Code

Pin Configurations

(TOP VIEW)



WQFN-48L 7x7

Ordering Information

CM501□□

- Package Type
  QW : WQFN-48L 7x7 (W-Type)
- Operating Temperature Range
  G : Green (Halogen Free with Commercial Standard)

Note :

Richtek Green products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

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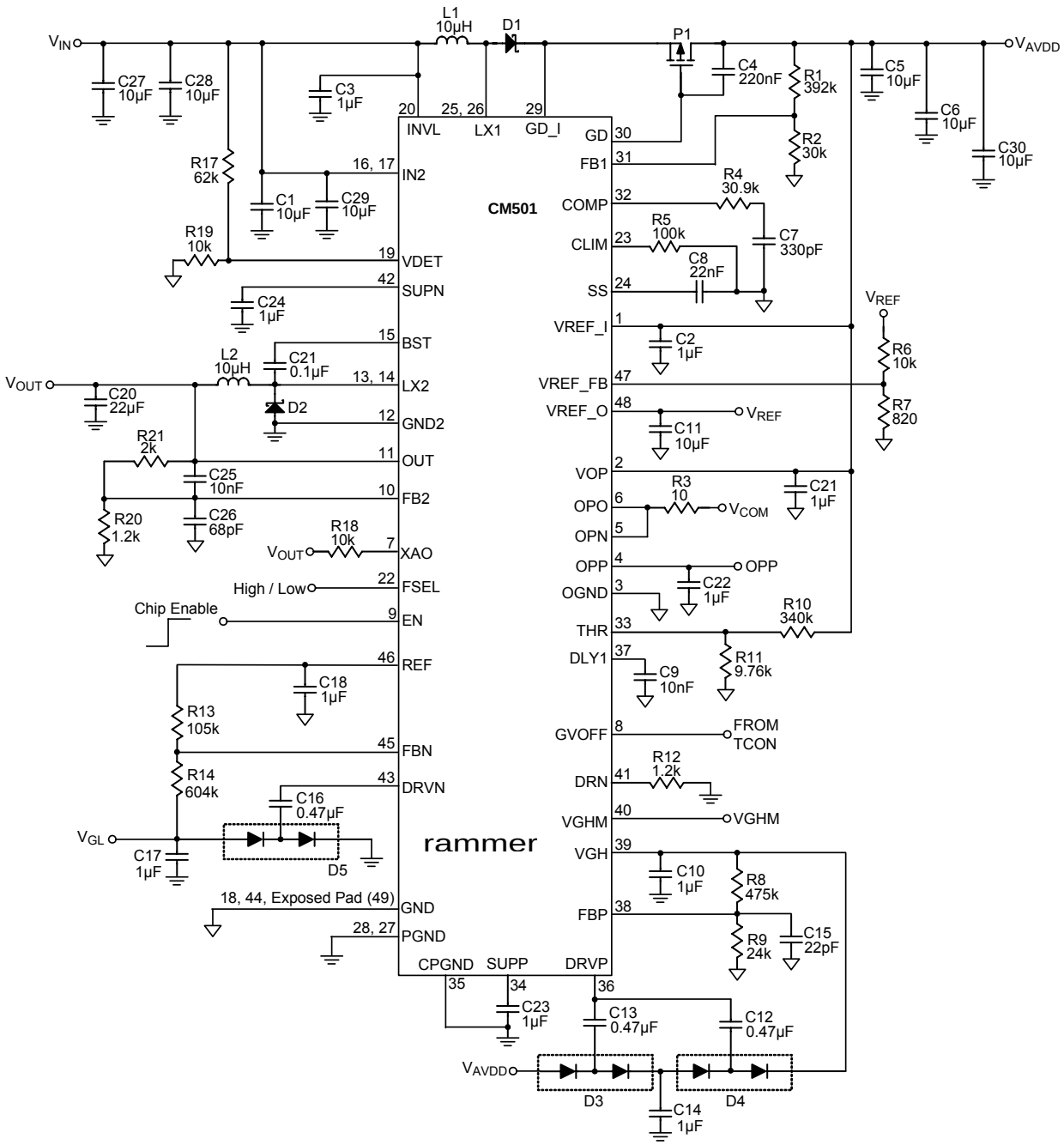
Typical Application Circuit



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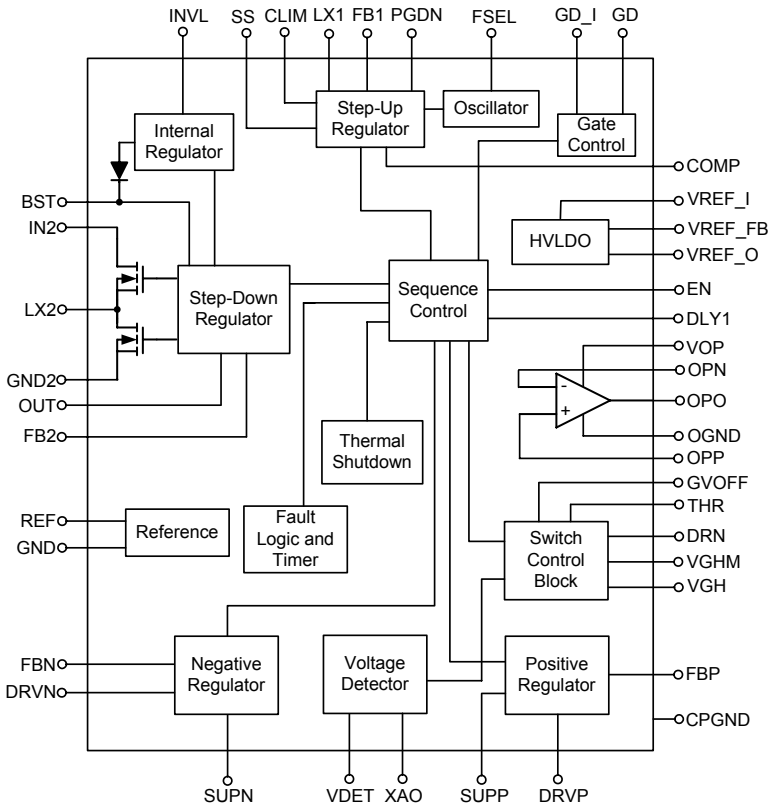
Function Block Diagram



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Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VREF_I	Linear Regulator Input. Bypass VREF_I to GND with a 1μF capacitor close to the pin.
2	VOP	Operational Amplifier Supply Input. Connect this pin to the output of boost regulator and bypass to OPGND with a 1μF capacitor.
3	OGND	Ground for Operational Amplifiers. Connect this pin to power ground underneath the IC.
4	OPP	Operational Amplifier Non-Inverting Input.
5	OPN	Operational Amplifier Inverting Input.
6	OPO	Operational Amplifier Output.
7	XAO	Reset Function Output.
8	GVOFF	High-Voltage Switch Control Input. When GVOFF is high, the high voltage switch between VGH and VGHM is on and the high-voltage switch between VGHM and DRN is off. When GVOFF is low, the switch between VGH and VGHM is off and the switch between VGHM and DRN is on. GVOFF is inhibited by the VIN under-voltage-lock-out when the voltage on DLY1 is less than 1.25V.
9	EN	Enable Input. Pulling EN high enables boost regulator and VGH charge pump.
10	FB2	Buck Regulator Feedback Input. Connect FB2 to the center of a resistive voltage-divider between buck regulator output and GND to set buck regulator output voltage.
11	OUT	Buck Regulator Output Sense Input. OUT is the inverting input to the internal current-sense amplifier. Connect OUT directly to the step-down regulator output.
12	GND2	Buck Regulator Power Ground.
13,14	LX2	Buck Regulator Switching Node. LX2 is the source of the internal high-side MOSFET. Connect the inductor and Schottky catch diode to LX2 and minimize the trace area for low EMI performance.
15	BST	Buck Regulator Bootstrap Pin. BST is the supply for the high-side MOSFET gate driver. Connect a 0.1μF ceramic capacitor from BST to LX2.
16,17	IN2	Buck Regulator Supply Input.
18	GND	Analog Ground.
19	VDET	Voltage Detection Input. Connect VDET to the center of a resistive voltage-divider between VIN and AGND.
20	INVL	4V Internal Linear Regulator and Startup Circuitry Supply Input. The input voltage range of INVL is between +8V and +14V. Connect a 1μF ceramic capacitor between INVL and GND. Place the capacitor close to the IC.
21	NC	No Internal Connection.
22	FSEL	Frequency Select Pin. Connect FSEL to VIN or leaving FSEL unconnected for 750kHz operation. Connect this pin to GND for 500kHz operation.
23	CLIM	Boost Regulator OCP level setting by an external resistor to GND.
24	SS	Soft-Start Control Pin. Connect a soft-start capacitor (C_{SS}) to this pin. Soft-start capacitor is charged with 5μA. The soft start capacitor is discharged to ground when EN is low. If C_{SS} is less than 200pF, soft-start is controlled internally and soft-start time is 10ms. Otherwise, the soft-start time is controlled by C_{SS} and 5μA charging current.
25,26	LX1	Boost Regulator Switching Node. Connect the inductor and the Schottky diode to LX1 and minimize the trace area for low EMI.
27,28	PGND	Boost Regulator Power Ground.

To be continued

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Pin No.	Pin Name	Pin Function
29	GD_I	Output sense pin. The GD_I pin is connected to the internal tracking circuit and over-voltage protection comparator. This pin needs to be connected to the output of the boost converter. Connect a 470nF capacitor from GD_I to GND to avoid noise coupling into this pin.
30	GD	This is the gate drive pin which can be used to control an external PMOSFET switch to provide input to output isolation of AVDD. GD pin will be pulled low when EN pulled high. GD pin pulled high when UVP/SCP is occurred.
31	FB1	Boost Regulator Feedback Input. Connect FB1 to the center of a resistive voltage-divider between boost regulator output and GND to set boost regulator output voltage. Place the resistive voltage-divider close to FB1.
32	COMP	Boost Regulator Error Amplifier Compensation Pin.
33	THR	VGHM Falling Regulation Adjustment Input. Connect THR to the center of a resistive voltage-divider between a reference supply and GND to adjust the VGHM falling regulation set point. GVOFF low allow VGHM to disconnect from VGH and be discharged through RE; discharge stops when VGHM reaches 10 x VTHR.
34	SUPP	VGH Charge-Pump Regulator Supply Input. Bypass SUPP to CPGND with a minimum 1μF ceramic capacitor.
35	CPGND	Power Ground for Charge Pump.
36	DRVP	VGH Charge-Pump Regulator Driver Output.
37	DLY1	VGH Charge-Pump Regulator and GPM Delay Input. Connect a capacitor between DLY1 and GND to set the delay time. A 5μA current source charges C_{DLY1}.
38	FBP	VGH Charge-Pump Regulator Feedback Input. Connect FBP to the center of a resistive voltage-divider between the positive output and GND to set the positive charge-pump regulator output voltage. Place the resistive voltage-divider close to FBP.
39	VGH	GPM Input.
40	VGHM	GPM Output.
41	DRN	GPM Discharge Pin.
42	SUPN	VGL Charge-Pump Regulator Supply Input. Bypass SUPN to GND with a minimum 1μF ceramic capacitor.
43	DRVN	VGL Charge-Pump Regulator Driver Output.
44	GND	VGL Charge-Pump Power Ground.
45	FBN	VGL Charge-Pump Regulator Feedback Input. Connect FBN to the center of a resistive voltage-divider between the negative output and REF to set the negative charge-pump regulator output voltage. Place the resistive voltage-divider close to FBN.
46	REF	Reference Output. Connect a 1μF ceramic capacitor between REF and GND.
47	VREF_FB	Linear Regulator Feedback Input. Connect VREF_FB to the center of a resistive voltage-divider between to VREF_O and AGND to set the needed regulator output voltage.
48	VREF_O	Linear Regulator output. Bypass VREF_O to GND with a minimum 1uF capacitor close to the pin.
49 (Exposed Pad)	GND	Ground Pin. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

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Absolute Maximum Ratings (Note 1)

- IN2, INVL, SUPN, FSEL to GND ---------- –0.3V to 16.5V
- SUPP, GD_I, VOP, VREF_I to GND ---------- –0.3V to 20V
- VOP to GND ---------- –0.3V to 20V
- DRVP tO CPGND ---------- –0.3V to (V_{SUPP} + 0.3V)
- DRVN to GND ---------- –0.3V to (V_{SUPN} + 0.3V)
- OPO, OPP, OPN to OGND ---------- –0.3V to (V_{VOP} + 0.3V)
- VREF_O to GND ---------- –0.3V to (V_{VREF_I} + 0.3V)
- FB1, FB2, FBP, FBN, GVOFF, DLY1, VREF_FB, THR, EN to GND ---------- –0.3V to 6.5V
- OUT, VL, REF, COMP, SS, XAO, VDEV, CLIM to GND ---------- –0.3V to 6.5V
- GD2, OPGND, CPGND to GND ---------- ±0.3V
- BST to GND2 ---------- –0.3V to 20V
- LX1 to PGND ---------- –0.3V to 20V
- LX2 to GND2 ---------- –0.3V to (IN2+0.3V)
- VGHM, VGH, DRN to GND ---------- –0.3V to 40V
- VGH to VGHM ---------- –0.3V to 40V
- VGH, VGHM to DRN ---------- –0.3V to 40V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-48L 7x7 ---------- 2.941W
- Package Thermal Resistance (Note 3)
  WQFN-48L 7x7, θ_{JA} ---------- 34°C/W
  WQFN-48L 7x7, θ_{JC} ---------- 7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C

Recommended Operating Conditions (Note 2)

- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
General						
IN2, INVL Input Voltage Range			8	12	14	V
Quiescent Current into INVL	I_{QIN}	LX not switching	--	0.02	2	mA
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} Falling	5.4	6	6.6	V
		Rising Hystersis	0.1	--	0.5	V
Switching Frequency		FSEL = GND	--	500	--	kHz
		FSEL = VIN	--	750	--	
Boost Regulator						
Maximum Duty Cycle			--	75	--	%
FB Regulation Voltage	V_{FB1}		-1	1.25	1%	V

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
FB Line Regulation		V_{IN} = 10.8V to 13.2V	--	0.15	0.2	%/V
Transconductance	G_m	△I = ±2.5μA at COMP = 1V	--	100	--	μA/V
Voltage Gain	A_V	FB to COMP	--	700	--	V/V
Current Limit	I_{LIM1}		3	4	--	A
On-Resistance	$R_{DS(ON)}$		--	100	250	mΩ
Current-Sense Transresistance	R_{CS}		--	0.25	--	V/A
Charge Current			--	5	--	μA
Internal Soft-Start		C_{SS} < 220pF	--	10	--	ms
Reference						
REF Output Voltage		No external load,	--	1.25	--	V
REF Load Regulation		0 < IREF < 50μA	--	10	--	mV
REF Sink Current		REF in Regulation	--	10	--	μA
Buck Regulator						
FB2 Regulation Voltage in Adjustable Mode	V_{FB2}		1.2375	1.25	1.2625	V
DC Line Regulation		10.8V < V_{IN} < 13.2V	--	0.1	--	%/V
LX2-to-IN2 Switch On-Resistance			--	150	300	mΩ
LX2-to-GND2 Switch On-Resistance			--	20	--	Ω
Current Limit			2.5	3.2	--	A
Error Amplifier Transconductance	G_{m2}		--	100	--	μA/V
Error Amplifier Voltage Gain	A_V		--	700	--	V/V
Current-Sense Transresistance	R_{CS}		--	0.3	--	V/A
Soft-Start Ramp Time			--	3	--	ms
FB2 UVP Trip Level		Falling edge	--	1	--	V
Duration to Trigger UVP Condition			--	50	--	ms
FB2 SCP Trip Level		Falling edge	--	0.5	--	V
Positive Charge-Pump Regulator						
FBP Regulation Voltage			1.225	1.25	1.275	V
FBP Line Regulation Error		V_{IN} = 10.8V to 13.2V	--	--	6	mV
DRVP P-MOSFET On-Resistance			--	4	--	Ω
DRVP N-MOSFET On-Resistance			--	1	--	Ω
Soft-Start Ramp Time			--	3	--	ms
FBP UVP Trip Level		Falling edge	--	1	--	V
Duration to Trigger Fault Condition			--	50	--	ms
FBP Short Circuit Level		Falling edge	--	0.5	--	V
Negative Charge-Pump Regulator						
FBN Regulation Voltage			0.21	0.25	0.29	V

To be continued

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
FBN Regulation Voltage		$V_{REF} - V_{FBN}$	0.98	1	1.02	V
FBN Line Regulation Error		V_{IN} = 10.8V to 13.2V	--	--	6	mV
DRVN P-MOSFET On-Resistance			--	4	--	Ω
DRVN N-MOSFET On-Resistance			--	1	--	Ω
Soft-Start Ramp Time			--	3	--	ms
FBN UVP Trip Level		$V_{REF} - V_{FBN}$	--	0.8	--	V
Duration to Trigger Fault Condition			--	50	--	ms
FBN Short Circuit Protection Level		$V_{REF} - V_{FBN}$	--	0.4	--	V
Sequence Control						
EN Input Low Voltage			--	--	0.6	V
EN Input High Voltage			1.5	--	5.5	V
DLY1 Capacitor Charge Current			--	5	--	μA
VDLY1 Turn-On Threshold			--	1.25	--	V
GD Output Sink Current		EN = High, $V_{GD\_I} = V_{IN}$	--	10	--	μA
GD On Voltage		EN = High, $V_{GD\_I} = V_{IN}$	--	$V_{IN} - 5$	--	V
Gate Pulse Modulator (GPM)						
GVOFF Input Low Voltage			--	--	0.6	V
GVOFF Input High Voltage			1.5	--	5.5	V
GVOFF Input Leakage Current			–1	--	1	μA
GVOFF -to-VGHM Rising Propagation Delay		1kΩ from DRN to GND, 1.5nF from VGHM to GND	--	100	--	ns
GVOFF to VGHM Falling Propagation Delay		1kΩ from DRN to GND, 1.5nF from VGHM to GND	--	250	--	ns
VGH Input Current		VDLY1 = GVOFF = 3V	--	1.5	2	mA
		VDLY1 = 3V, GVOFF = 0	--	0.14	0.2	
DRN Input Current		DRN = 8V, VDLY1 = 3V, VGHM > DRN, GVOFF = 0	--	0	1	μA
VGH Switch On-Resistance		VDLY1 = GVOFF = 3V	--	5	10	Ω
DRN Switch On-Resistance		VDLY1 = 3V, GVOFF = 0, VGHM= 28V, THR = 1.4V	--	20	50	Ω
THR to VGHM Voltage Gain			--	10	--	V/V
Voltage Detector (XAO)						
Detecting Voltage Adjustment	V_{DET}	Falling edge	--	1.25	--	V
Detecting Voltage Accuracy			–1	--	1	%
VCOMP OP						
Supply Current	I_{OP}		--	3	--	mA
Input Offset Voltage	V_{OS}	V_{COM} = AVDD/2	--	--	20	mV
Input Bias Current	I_{BIAS}		--	1	100	nA
Output Voltage Swing High	V_{OH}	I_{LOAD} = 10mA	--	V_{SUP} –100	--	mV

To be continued

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage Swing Low	V_{OL}	I_{LOAD} = –10mA	--	100	--	mV
Short-Circuit Current		To AVDD/2 Source or Sink for 1ms	--	300	--	mA
-3dB Bandwidth	F_{3dB}	R_L = 10kΩ, C_L = 10pF	--	20	--	MHz
Gain Bandwidth Product	G_{BW}	R_L = 10kΩ, C_L = 10pF	--	8	--	MHz
Slew Rate			--	45	--	V/μs
HVLDO						
Quiescent Current	I_Q		--	40	--	μA
Feedback Voltage			--	1.25	--	V
Feedback Voltage Tolerance			–0.5	--	0.5	%
Output Current Limit		V_{REF_I} = 15V, V_{REF_O} = 14V, R_{OUT} = 50Ω	60	--	--	mA
Dropout Voltage		I_{LOAD} = 60mA	--	0.5	--	V
Power Supply Rejection Rate		V_{REF_I} = V_{REF_O} + 1V, I_{OUT} = 10mA	--	60	--	dB
Protection						
Thermal Shutdown Threshold	T_{SD}		--	160	--	°C
Switching-Frequency Selection						
FSEL Input Levels		FSEL = V_{IN} (750kHz), High	1.5	--	--	V
		FSEL = GND (500kHz), Low	--	--	0.6	
FSEL Pull High Current			--	5	--	μA

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. The device is not guaranteed to function outside its operating conditions.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective thermal conductivity four layers test board.

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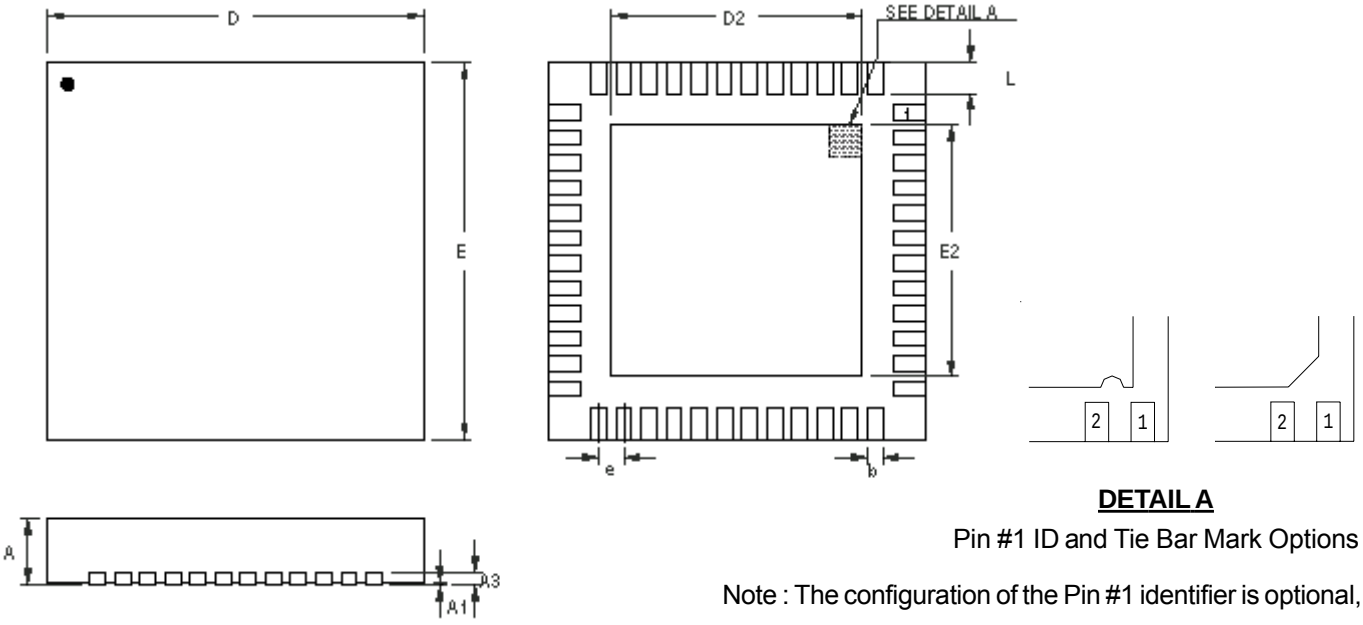
Outline Dimension



DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	6.950	7.050	0.274	0.278
D2	5.050	5.250	0.199	0.207
E	6.950	7.050	0.274	0.278
E2	5.050	5.250	0.199	0.207
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 48L QFN 7x7 Package

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Datasheet Revision History

Version	Data	Page No.	Item	Description
P00T00	2009/10/5			first edition
P00T00	2009/10/7		Features Typical Application Circuit Function Block Diagram Electrical Characteristics	Modify