# MCP6021/2/3/4

## Rail-to-Rail Input/Output, 10 MHz Op Amps

### Features

- Rail-to-Rail Input/Output
- Wide Bandwidth: 10 MHz (typ.)
- Low Noise: 8.7 nV/√Hz, at 10 kHz (typ.)
- Low Offset Voltage:
  - Industrial Temperature: ±500 µV (max.)
  - Extended Temperature: ±250 µV (max.)
- Mid-Supply $V_{REF}$: MCP6021 and MCP6023
- Low Supply Current: 1 mA (typ.)
- Total Harmonic Distortion: 0.00053% (typ., G = 1)
- Unity Gain Stable
- Power Supply Range: 2.5V to 5.5V
- Temperature Range:
  - Industrial: -40°C to +85°C
  - Extended: -40°C to +125°C

### Typical Applications

- Automotive
- Driving A/D Converters
- Multi-Pole Active Filters
- Barcode Scanners
- Audio Processing
- Communications
- DAC Buffer
- Test Equipment
- Medical Instrumentation

### Available Tools

- SPICE Macro Model (at www.microchip.com)
- FilterLab® software (at www.microchip.com)

### Description

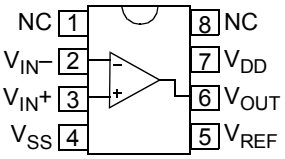
The MCP6021, MCP6022, MCP6023 and MCP6024 from Microchip Technology Inc. are rail-to-rail input and output op amps with high performance. Key specifications include: wide bandwidth (10 MHz), low noise (8.7 nV/√Hz), low input offset voltage and low distortion (0.00053% THD+N). These features make these op amps well suited for applications requiring high performance and bandwidth. The MCP6023 also offers a chip select pin ($\overline{CS}$) that gives power savings when the part is not in use.

The single MCP6021, single MCP6023 and dual MCP6022 are available in standard 8-lead PDIP, SOIC and TSSOP. The quad MCP6024 is offered in 14-lead PDIP, SOIC and TSSOP packages.

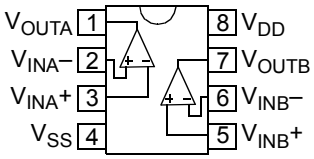
The MCP6021/2/3/4 family is available in the Industrial and Extended temperature ranges. It has a power supply range of 2.5V to 5.5V.

## PACKAGE TYPES

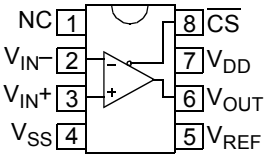
**MCP6021**
**PDIP SOIC, TSSOP**



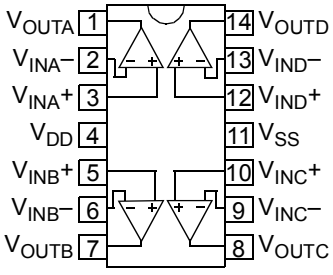

**MCP6022**
**PDIP SOIC, TSSOP**




**MCP6023**
**PDIP SOIC, TSSOP**




**MCP6024**
**PDIP SOIC, TSSOP**



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

$V_{DD}$ - $V_{SS}$ .....7.0V
All Inputs and Outputs..... $V_{SS}$ - 0.3V to $V_{DD}$ + 0.3V
Difference Input Voltage ..... $|V_{DD} - V_{SS}|$
Output Short Circuit Current .....continuous
Current at Input Pins .....±2 mA
Current at Output and Supply Pins .....±30 mA
Storage Temperature .....-65°C to +150°C
Junction Temperature.....+150°C
ESD Protection on all pins (HBM/MM) ..... ≥ 2 kV / 200V

**† Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

### Pin Function Table

| Name | Function |
|---|---|
| $V_{IN}+$, $V_{INA}+$, $V_{INB}+$, $V_{INC}+$, $V_{IND}+$ | Non-inverting Inputs |
| $V_{IN}–$, $V_{INA}–$, $V_{INB}–$, $V_{INC}–$, $V_{IND}–$ | Inverting Inputs |
| $V_{DD}$ | Positive Power Supply |
| $V_{SS}$ | Negative Power Supply |
| $\overline{CS}$ | Chip Select |
| $V_{REF}$ | Reference Voltage |
| $V_{OUT}$, $V_{OUTA}$, $V_{OUTB}$, $V_{OUTC}$, $V_{OUTD}$ | Outputs |
| NC | No Internal Connection |

## DC CHARACTERISTICS

**Electrical Specifications:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = +2.5V to +5.5V, $V_{SS}$ = GND, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$ and $R_L$ = 10 kΩ to $V_{DD}/2$.

| Parameters | Sym | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **Input Offset** | | | | | | |
| Input Offset Voltage: | | | | | | |
| Industrial Temperature Parts | $V_{OS}$ | -500 | — | +500 | µV | $V_{CM}$ = 0V |
| Extended Temperature Parts | $V_{OS}$ | -250 | — | +250 | µV | $V_{CM}$ = 0V, $V_{DD}$ = 5.0V |
| Extended Temperature Parts | $V_{OS}$ | -2.5 | — | +2.5 | mV | $V_{CM}$ = 0V, $V_{DD}$ = 5.0V<br>$T_A$ = -40°C to +125°C |
| Input Offset Voltage Temperature Drift | $\Delta V_{OS}/\Delta T_A$ | — | ±3.5 | — | µV/°C | $T_A$ = -40°C to +125°C |
| Power Supply Rejection Ratio | PSRR | 74 | 90 | — | dB | $V_{CM}$ = 0V |
| **Input Current and Impedance** | | | | | | |
| Input Bias Current | $I_B$ | — | 1 | — | pA | |
| Industrial Temperature Parts | $I_B$ | — | 30 | 150 | pA | $T_A$ = +85°C |
| Extended Temperature Parts | $I_B$ | — | 640 | 5,000 | pA | $T_A$ = +125°C |
| Input Offset Current | $I_{OS}$ | — | ±1 | — | pA | |
| Common-Mode Input Impedance | $Z_{CM}$ | — | $10^{13}$\|\|6 | — | Ω\|\|pF | |
| Differential Input Impedance | $Z_{DIFF}$ | — | $10^{13}$\|\|3 | — | Ω\|\|pF | |
| **Common-Mode** | | | | | | |
| Common-Mode Input Range | $V_{CMR}$ | $V_{SS}$-0.3 | — | $V_{DD}$+0.3 | V | |
| Common-Mode Rejection Ratio | CMRR | 74 | 90 | — | dB | $V_{DD}$ = 5V, $V_{CM}$ = -0.3V to 5.3V |
| | CMRR | 70 | 85 | — | dB | $V_{DD}$ = 5V, $V_{CM}$ = 3.0V to 5.3V |
| | CMRR | 74 | 90 | — | dB | $V_{DD}$ = 5V, $V_{CM}$ = -0.3V to 3.0V |
| **Voltage Reference (MCP6021 and MCP6023 only)** | | | | | | |
| $V_{REF}$ Accuracy ($V_{REF}$ - $V_{DD}/2$) | $\Delta V_{REF}$ | -50 | — | +50 | mV | |
| $V_{REF}$ Temperature Drift | $\Delta V_{REF}/\Delta T_A$ | — | ±100 | — | µV/°C | $T_A$ = -40°C to +125°C |
| Open Loop Gain | | | | | | |
| DC Open Loop Gain (Large Signal) | $A_{OL}$ | 90 | 110 | — | dB | $V_{CM}$ = 0V,<br>$V_{OUT}$ = $V_{SS}$+0.3V to $V_{DD}$-0.3V |

## DC CHARACTERISTICS (CONTINUED)

**Electrical Specifications:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = +2.5V to +5.5V, $V_{SS}$ = GND, $V_{CM}$ = $V_{DD}$/2, $V_{OUT}$ ≈ $V_{DD}$/2 and $R_L$ = 10 kΩ to $V_{DD}$/2.

| Parameters | Sym | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **Output** | | | | | | |
| Maximum Output Voltage Swing | $V_{OL}$, $V_{OH}$ | $V_{SS}$+15 | — | $V_{DD}$-20 | mV | 0.5V output overdrive |
| Output Short Circuit Current | $I_{SC}$ | — | ±30 | — | mA | |
| **Power Supply** | | | | | | |
| Supply Voltage | $V_S$ | 2.5 | — | 5.5 | V | |
| Quiescent Current per Amplifier | $I_Q$ | 0.5 | 1.0 | 1.35 | mA | $I_O$ = 0 |

## AC CHARACTERISTICS

**Electrical Specifications:** Unless otherwise indicated, $T_A$ = 25°C, $V_{DD}$ = +2.5V to +5.5V, $V_{SS}$ = GND, $V_{CM}$ = $V_{DD}$/2, $V_{OUT}$ ≈ $V_{DD}$/2, $R_L$ = 10 kΩ to $V_{DD}$/2 and $C_L$ = 60 pF.

| Parameters | Sym | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **AC Response** | | | | | | |
| Gain Bandwidth Product | GBWP | — | 10 | — | MHz | |
| Phase Margin at Unity-Gain | PM | — | 65 | — | ° | G = 1 |
| Settling Time, 0.2% | $t_{SETTLE}$ | — | 250 | — | ns | G = 1, $V_{OUT}$ = 100 $mV_{p-p}$ |
| Slew Rate | SR | — | 7.0 | — | V/µs | |
| **Total Harmonic Distortion Plus Noise** | | | | | | |
| f = 1 kHz, G = 1 | THD+N | — | 0.00053 | — | % | $V_{OUT}$ = 0.25V + 3.25V, BW = 22 kHz |
| f = 1 kHz, G = 1, $R_L$ = 600Ω@1 KHz | THD+N | — | 0.00064 | — | % | $V_{OUT}$ = 0.25V + 3.25V, BW = 22 kHz |
| f = 1 kHz, G = +1 V/V | THD+N | — | 0.0014 | — | % | $V_{OUT}$ = $4V_{P-P}$, $V_{DD}$ = 5.0V, BW = 22 kHz |
| f = 1 kHz, G = +10 V/V | THD+N | — | 0.0009 | — | % | $V_{OUT}$ = $4V_{P-P}$, $V_{DD}$ = 5.0V, BW = 22 kHz |
| f = 1 kHz, G = +100 V/V | THD+N | — | 0.005 | — | % | $V_{OUT}$ = $4V_{P-P}$, $V_{DD}$ = 5.0V, BW = 22 kHz |
| **Noise** | | | | | | |
| Input Voltage Noise | $E_{ni}$ | — | 2.9 | — | µVp-p | f = 0.1 Hz to 10 Hz |
| Input Voltage Noise Density | $e_{ni}$ | — | 8.7 | — | nV/√Hz | f = 10 kHz |
| Input Current Noise Density | $i_{ni}$ | — | 3 | — | fA/√Hz | f = 1 kHz |

## MCP6023 CHIP SELECT ($\overline{CS}$) CHARACTERISTICS

**Electrical Specifications:** Unless otherwise indicated, $T_A$ = 25°C, $V_{DD}$ = +2.5V to +5.5V, $V_{SS}$ = GND, $V_{CM}$ = $V_{DD}$/2, $V_{OUT}$ ≈ $V_{DD}$/2, $R_L$ = 10 kΩ to $V_{DD}$/2 and $C_L$ = 60 pF.

| Parameters | Sym | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **DC Characteristics** | | | | | | |
| $\overline{CS}$ Logic Threshold, Low | $V_{IL}$ | 0 | — | 0.2$V_{DD}$ | V | |
| $\overline{CS}$ Input Current, Low | $I_{CSL}$ | -1.0 | 0.01 | — | µA | $\overline{CS}$ = $V_{SS}$ |
| $\overline{CS}$ Logic Threshold, High | $V_{IH}$ | 0.8$V_{DD}$ | — | $V_{DD}$ | V | |
| $\overline{CS}$ Input Current, High | $I_{CSH}$ | — | 0.01 | 2.0 | µA | $\overline{CS}$ = $V_{DD}$ |
| $\overline{CS}$ Input High, GND Current | $I_{SS}$ | — | 0.05 | 2.0 | µA | $\overline{CS}$ = $V_{DD}$ |
| Amplifier Output Leakage | — | — | 0.01 | — | µA | $\overline{CS}$ = $V_{DD}$ |
| **Timing** | | | | | | |
| $\overline{CS}$ Low to Amplifier Output Turn-on Time | $t_{ON}$ | — | 2 | 10 | µs | G = 1, $V_{IN}$ = $V_{SS}$, $\overline{CS}$ = 0.2$V_{DD}$ to $V_{OUT}$ = 0.45$V_{DD}$ time |
| $\overline{CS}$ High to Amplifier Output High-Z Turn-off Time | $t_{OFF}$ | — | 0.01 | — | µs | G = 1, $V_{IN}$ = $V_{SS}$, $\overline{CS}$ = 0.8$V_{DD}$ to $V_{OUT}$ = 0.05$V_{DD}$ time |
| Hysteresis | $V_{HYST}$ | — | 0.6 | — | V | Internal Switch |

## TEMPERATURE CHARACTERISTICS

| **Electrical Specifications:** Unless otherwise indicated, $V_{DD}$ = +2.5V to +5.5V and $V_{SS}$ = GND. | | | | | | |
|---|---|---|---|---|---|---|
| **Parameters** | **Symbol** | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| **Temperature Ranges** | | | | | | |
| Industrial Temperature Range | $T_A$ | -40 | — | +85 | °C | |
| Extended Temperature Range | $T_A$ | -40 | — | +125 | °C | |
| Operating Temperature Range | $T_A$ | -40 | — | +125 | °C | **Note 1** |
| Storage Temperature Range | $T_A$ | -65 | — | +150 | °C | |
| **Thermal Package Resistances** | | | | | | |
| Thermal Resistance, 8L-PDIP | $\theta_{JA}$ | — | 85 | — | °C/W | |
| Thermal Resistance, 8L-SOIC | $\theta_{JA}$ | — | 163 | — | °C/W | |
| Thermal Resistance, 8L-TSSOP | $\theta_{JA}$ | — | 124 | — | °C/W | |
| Thermal Resistance, 14L-PDIP | $\theta_{JA}$ | — | 70 | — | °C/W | |
| Thermal Resistance, 14L-SOIC | $\theta_{JA}$ | — | 120 | — | °C/W | |
| Thermal Resistance, 14L-TSSOP | $\theta_{JA}$ | — | 100 | — | °C/W | |

**Note 1:** The industrial temperature devices operate over this extended temperature range, but with reduced performance. In any case, the internal junction temperature ($T_J$) must not exceed the absolute maximum specification of 150°C.

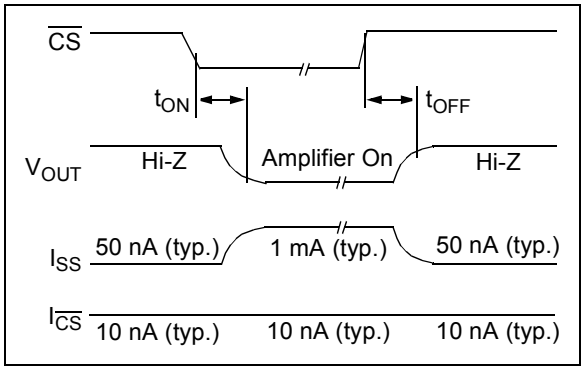



***FIGURE 1-1:*** *Timing diagram for the $\overline{CS}$ pin on the MCP6023.*

## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = +2.5V to +5.5V, $V_{SS}$ = GND, $V_{CM}$ = $V_{DD}$/2, $R_L$ = 10 kΩ to $V_{DD}$/2, $V_{OUT} \approx V_{DD}/2$ and $C_L$ = 60 pF.

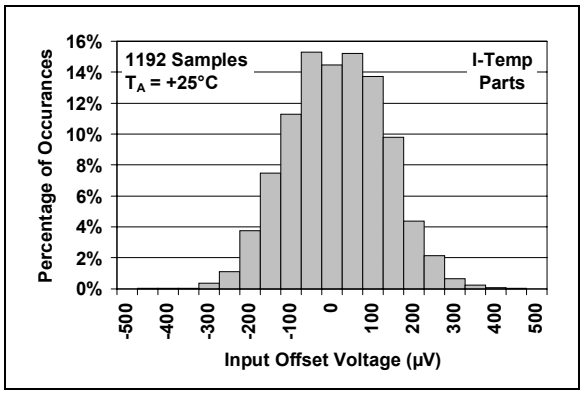



***FIGURE 2-1:*** *Input Offset Voltage, (Industrial Temperature Parts).*

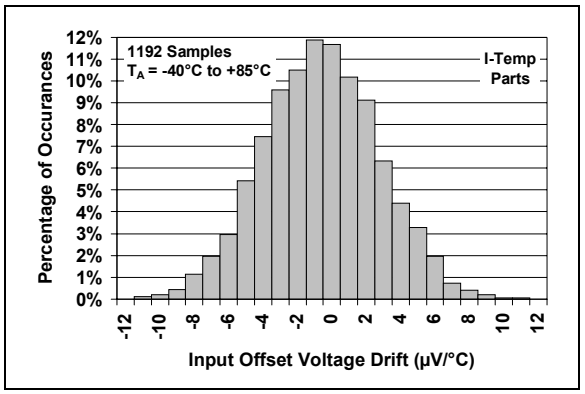



***FIGURE 2-4:*** *Input Offset Voltage Drift, (Industrial Temperature Parts).*

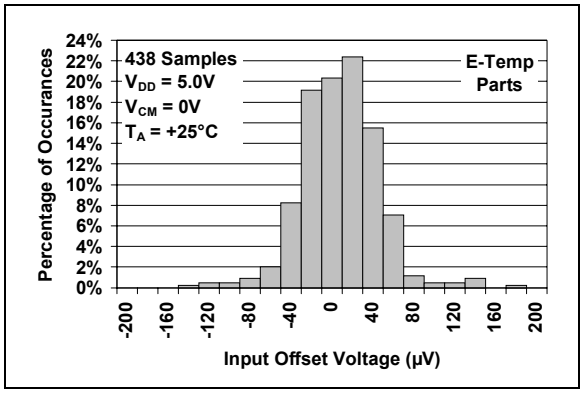



***FIGURE 2-2:*** *Input Offset Voltage, (Extended Temperature Parts).*

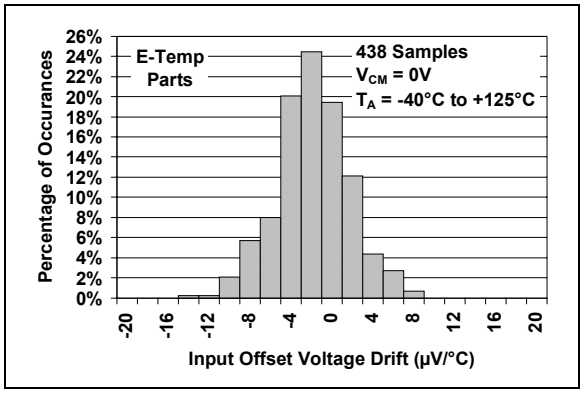



***FIGURE 2-5:*** *Input Offset Voltage Drift, (Extended Temperature Parts).*

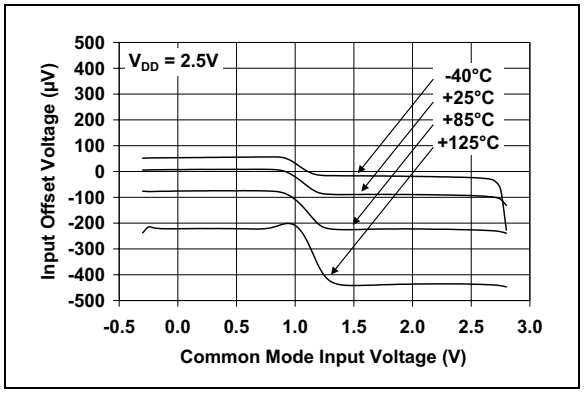



***FIGURE 2-3:*** *Input Offset Voltage vs. Common Mode Input Voltage with $V_{DD}$ = 2.5V.*

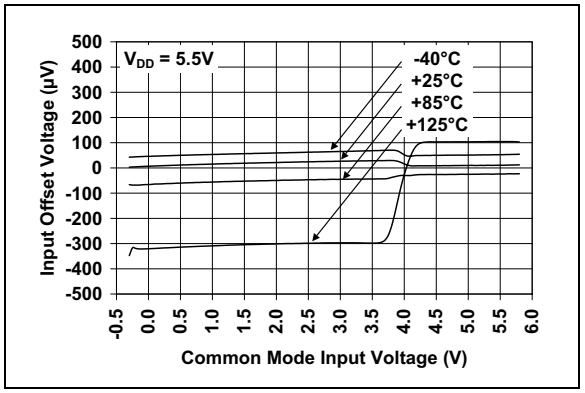



***FIGURE 2-6:*** *Input Offset Voltage vs. Common Mode Input Voltage with $V_{DD}$ = 5.5V.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = +2.5V to +5.5V, $V_{SS}$ = GND, $V_{CM}$ = $V_{DD}$/2, $R_L$ = 10 kΩ to $V_{DD}$/2, $V_{OUT} \approx V_{DD}/2$ and $C_L$ = 60 pF.

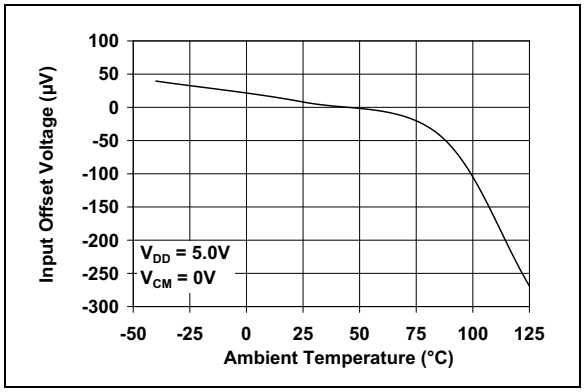



***FIGURE 2-7:*** *Input Offset Voltage vs. Temperature.*

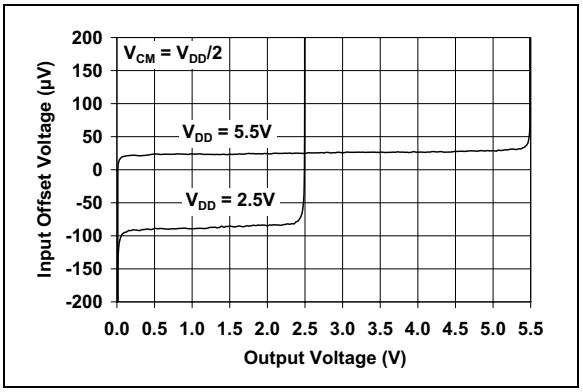



***FIGURE 2-10:*** *Input Offset Voltage vs. Output Voltage.*

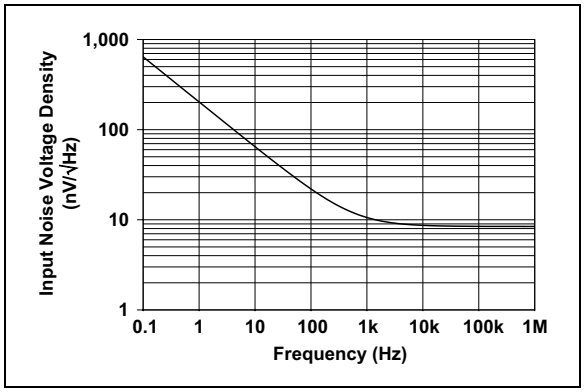



***FIGURE 2-8:*** *Input Noise Voltage Density vs. Frequency.*

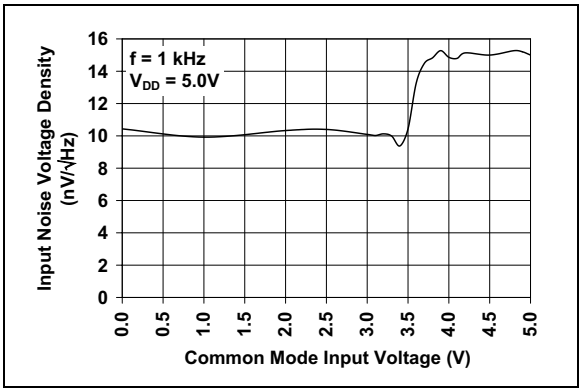



***FIGURE 2-11:*** *Input Noise Voltage Density vs. Common Mode Input Voltage.*

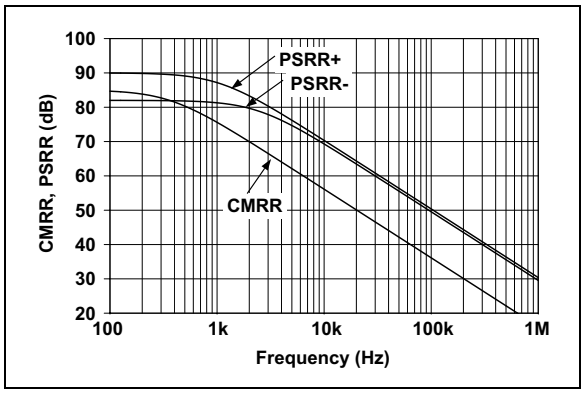



***FIGURE 2-9:*** *Common Mode, Power Supply Rejection Ratios vs. Frequency.*

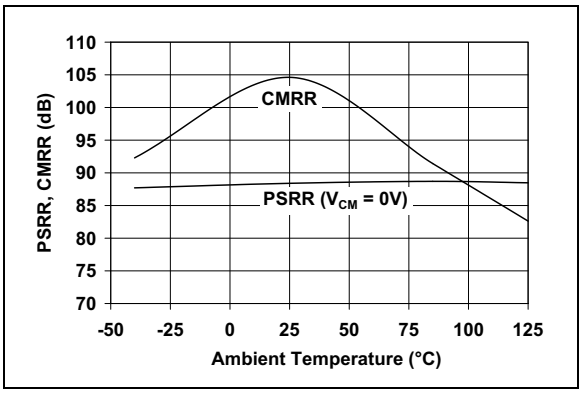



***FIGURE 2-12:*** *Common Mode, Power Supply Rejection Ratios vs. Temperature.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = +2.5V to +5.5V, $V_{SS}$ = GND, $V_{CM}$ = $V_{DD}$/2, $R_L$ = 10 kΩ to $V_{DD}$/2, $V_{OUT} \approx V_{DD}/2$ and $C_L$ = 60 pF.

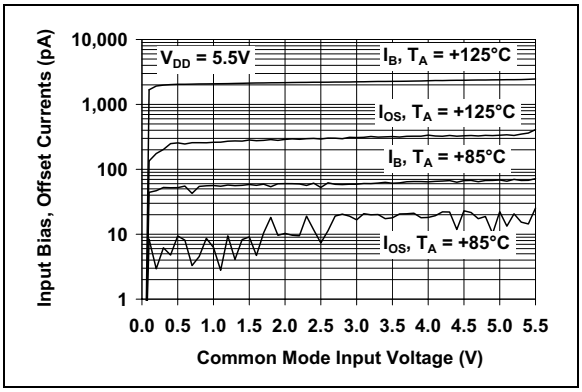



***FIGURE 2-13:*** *Input Bias, Offset Currents vs. Common Mode Input Voltage.*

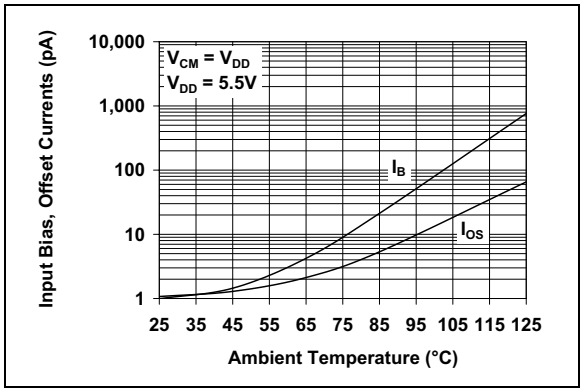



***FIGURE 2-16:*** *Input Bias, Offset Currents vs. Temperature.*

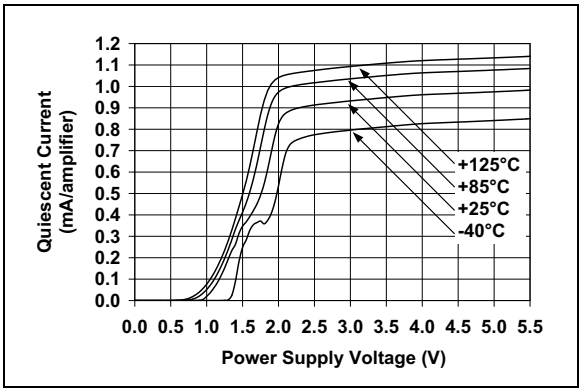



***FIGURE 2-14:*** *Quiescent Current vs. Supply Voltage.*

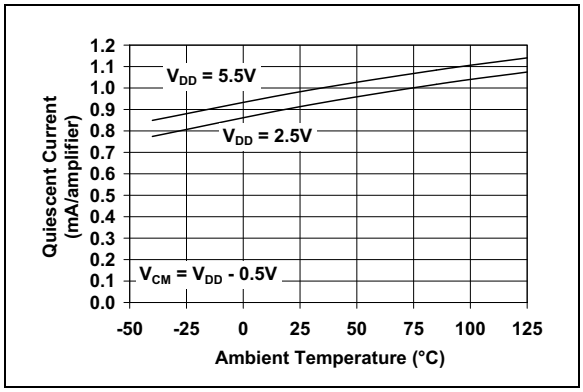



***FIGURE 2-17:*** *Quiescent Current vs. Temperature.*

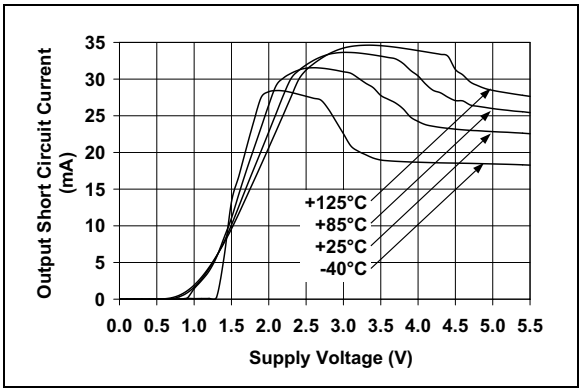



***FIGURE 2-15:*** *Output Short-Circuit Current vs. Supply Voltage.*

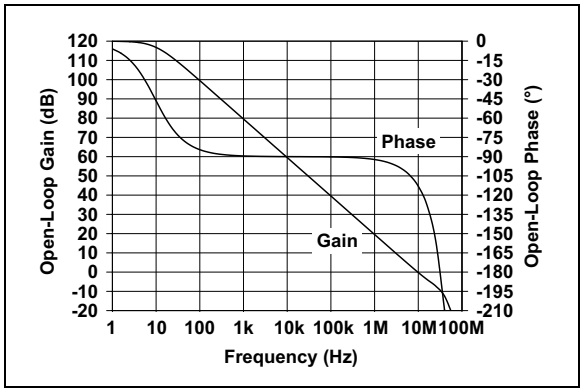



***FIGURE 2-18:*** *Open-Loop Gain, Phase vs. Frequency.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = +2.5V to +5.5V, $V_{SS}$ = GND, $V_{CM}$ = $V_{DD}$/2, $R_L$ = 10 kΩ to $V_{DD}$/2, $V_{OUT} \approx V_{DD}/2$ and $C_L$ = 60 pF.

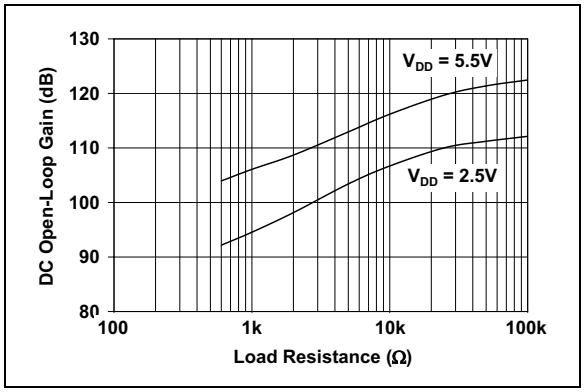



***FIGURE 2-19:*** *DC Open-Loop Gain vs. Load Resistance.*

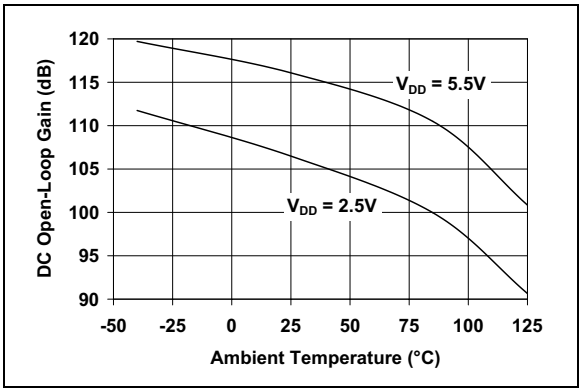



***FIGURE 2-22:*** *DC Open-Loop Gain vs. Temperature.*

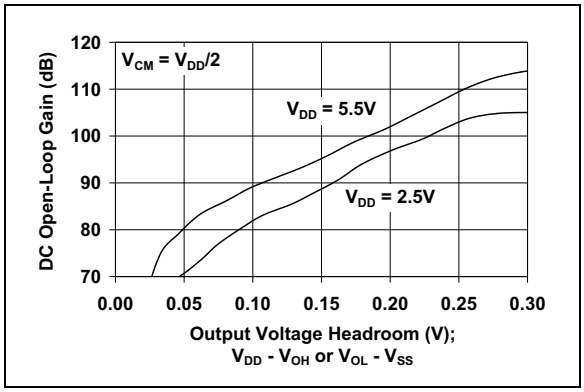



***FIGURE 2-20:*** *Small Signal DC Open-Loop Gain vs. Output Voltage Headroom.*

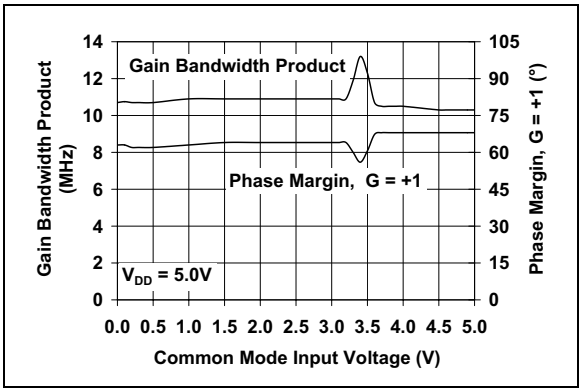



***FIGURE 2-23:*** *Gain Bandwidth Product, Phase Margin vs. Common Mode Input Voltage.*

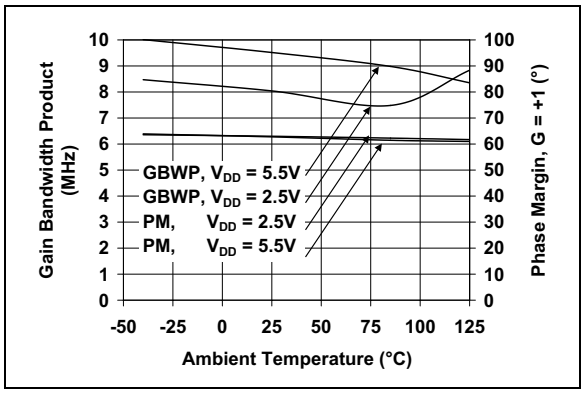



***FIGURE 2-21:*** *Gain Bandwidth Product, Phase Margin vs. Temperature.*

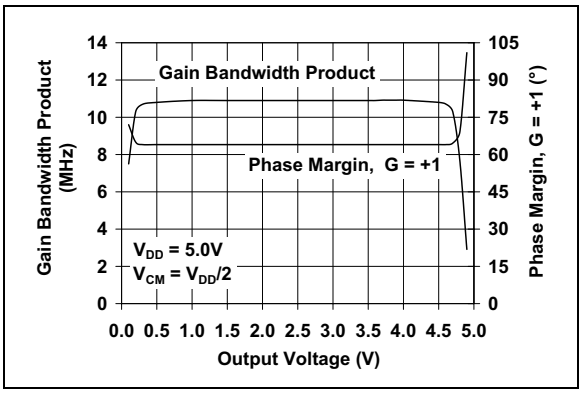



***FIGURE 2-24:*** *Gain Bandwidth Product, Phase Margin vs. Output Voltage.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = +2.5V to +5.5V, $V_{SS}$ = GND, $V_{CM}$ = $V_{DD}$/2, $R_L$ = 10 kΩ to $V_{DD}$/2, $V_{OUT}$ ≈ $V_{DD}$/2 and $C_L$ = 60 pF.

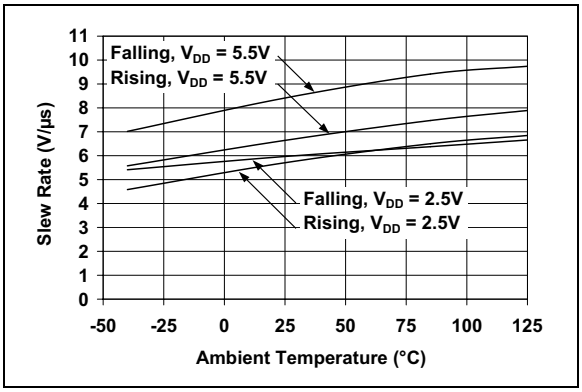



***FIGURE 2-25:*** *Slew Rate vs. Temperature.*

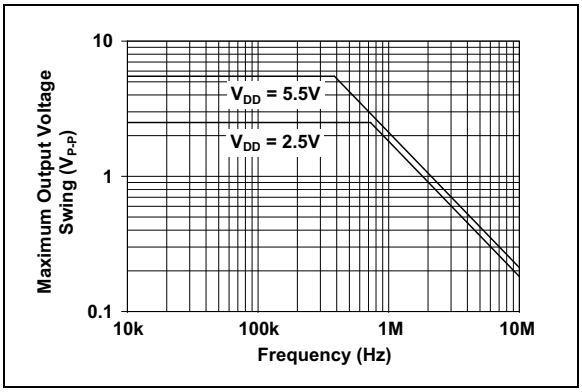



***FIGURE 2-28:*** *Maximum Output Voltage Swing vs. Frequency.*

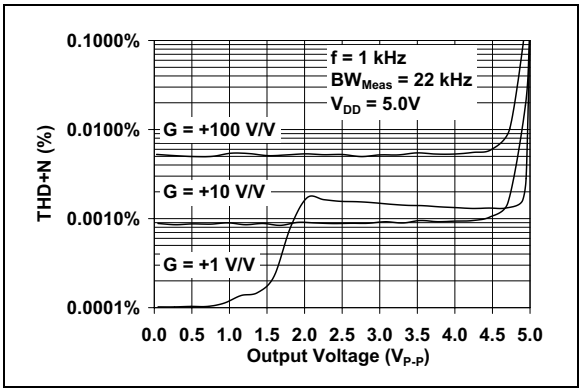



***FIGURE 2-26:*** *Total Harmonic Distortion plus Noise vs. Output Voltage with f = 1 kHz.*

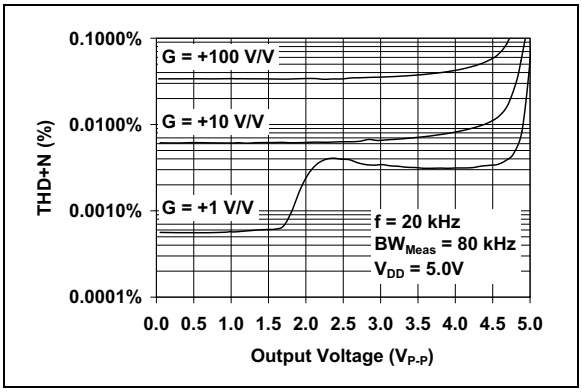



***FIGURE 2-29:*** *Total Harmonic Distortion plus Noise vs. Output Voltage with f = 20 kHz.*

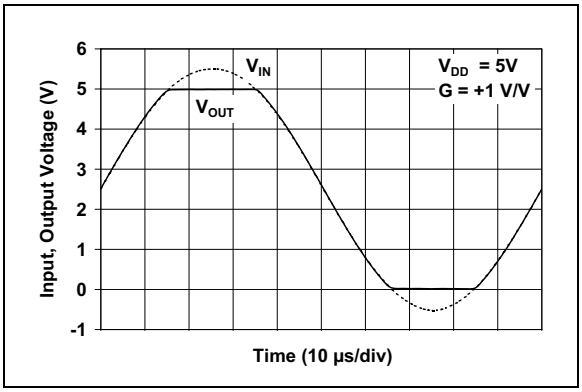



***FIGURE 2-27:*** *The MCP6021/2/3/4 family shows no phase reversal under overdrive.*

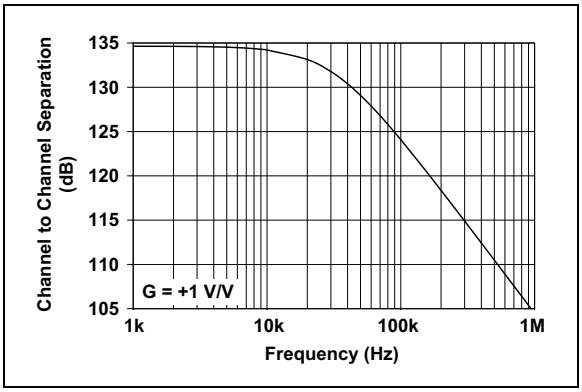



***FIGURE 2-30:*** *Channel-to-Channel Separation vs. Frequency (MCP6022 and MCP6024 only).*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = +2.5V to +5.5V, $V_{SS}$ = GND, $V_{CM}$ = $V_{DD}$/2, $R_L$ = 10 kΩ to $V_{DD}$/2, $V_{OUT} \approx V_{DD}/2$ and $C_L$ = 60 pF.

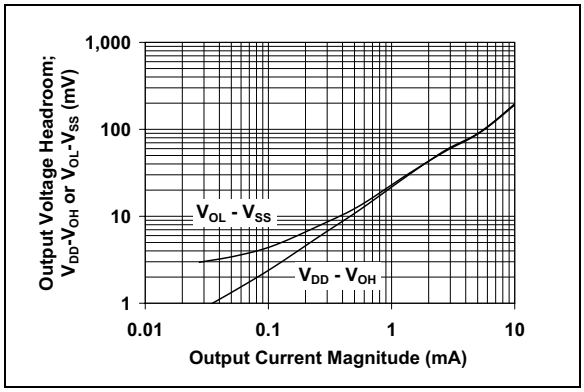



***FIGURE 2-31:*** *Output Voltage Headroom vs. Output Current.*

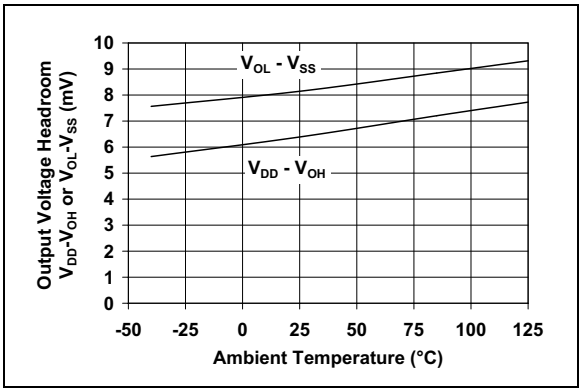



***FIGURE 2-34:*** *Output Voltage Headroom vs. Temperature.*

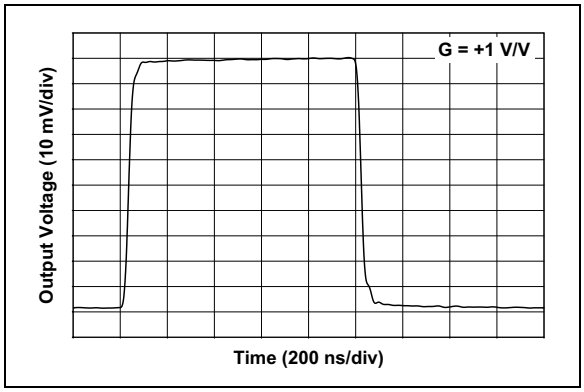



***FIGURE 2-32:*** *Small-Signal Non-inverting Pulse Response.*

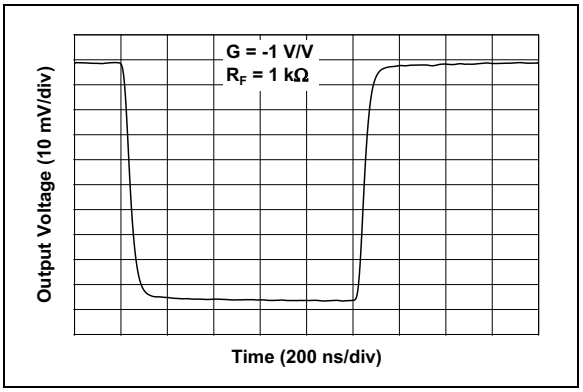



***FIGURE 2-35:*** *Small-Signal Inverting Pulse Response.*

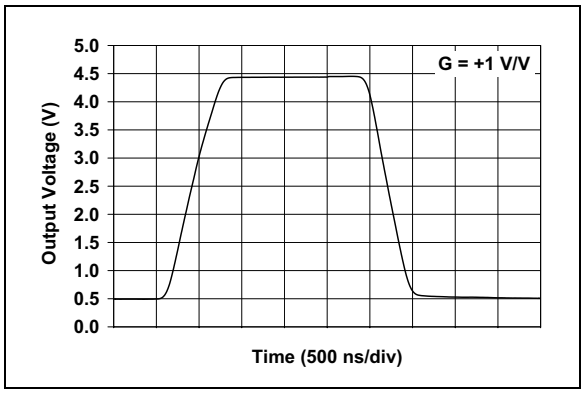



***FIGURE 2-33:*** *Large-Signal Non-inverting Pulse Response.*

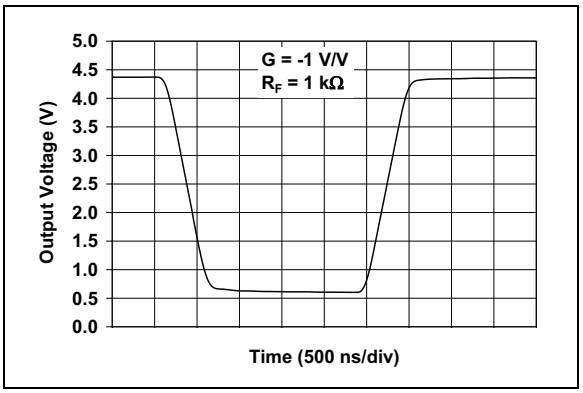



***FIGURE 2-36:*** *Large-Signal Inverting Pulse Response.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = +2.5V to +5.5V, $V_{SS}$ = GND, $V_{CM}$ = $V_{DD}$/2, $R_L$ = 10 kΩ to $V_{DD}$/2, $V_{OUT} \approx V_{DD}/2$ and $C_L$ = 60 pF.

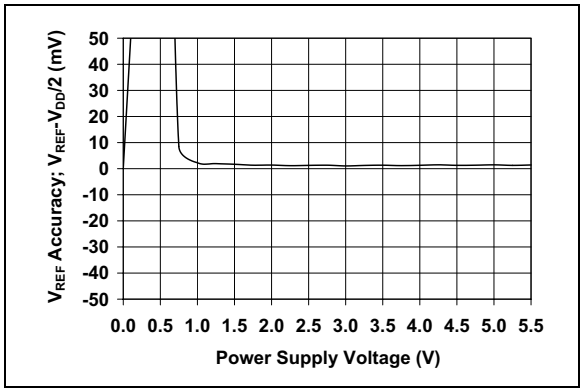



***FIGURE 2-37:*** *$V_{REF}$ Accuracy vs. Supply Voltage (MCP6021 and MCP6023 only).*

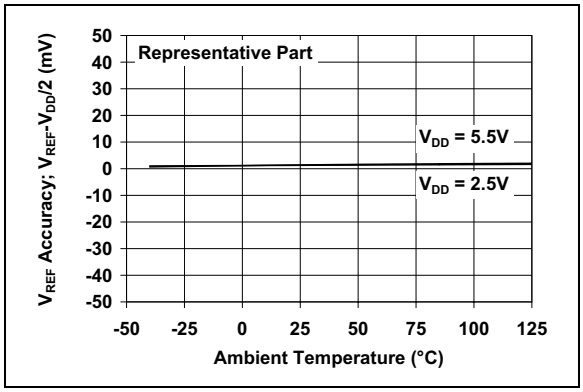



***FIGURE 2-40:*** *$V_{REF}$ Accuracy vs. Temperature (MCP6021 and MCP6023 only).*

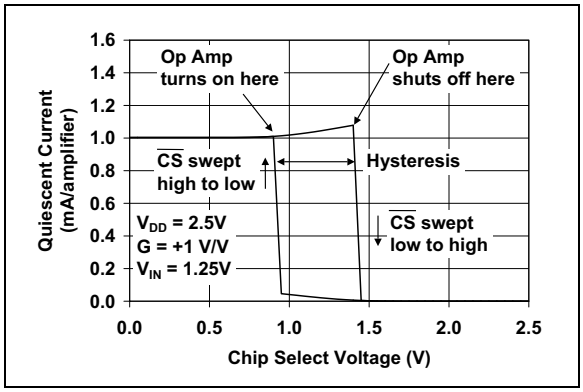



***FIGURE 2-38:*** *Chip Select ($\overline{CS}$) Hysteresis (MCP6023 only) with $V_{DD}$ = 2.5V.*

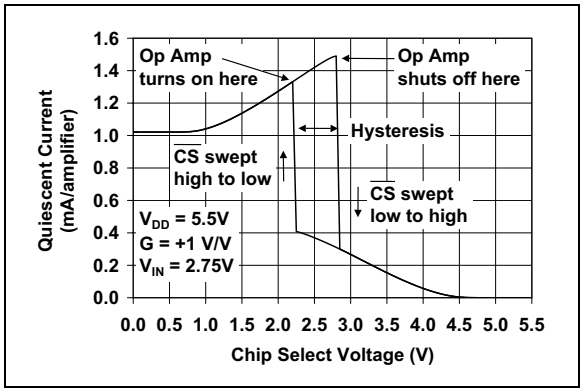



***FIGURE 2-41:*** *Chip Select ($\overline{CS}$) Hysteresis (MCP6023 only) with $V_{DD}$ = 5.5V.*

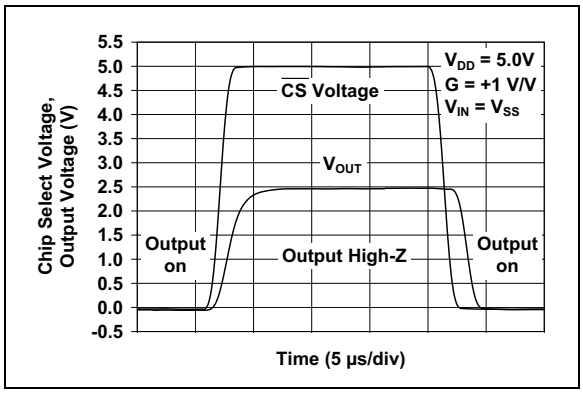



***FIGURE 2-39:*** *Chip Select ($\overline{CS}$) to Amplifier Output Response Time (MCP6023 only).*

## 3.0 APPLICATIONS INFORMATION

The MCP6021/2/3/4 family of operational amplifiers are fabricated on Microchip's state-of-the-art CMOS process. They are unity-gain stable and suitable for a wide range of general-purpose applications.

### 3.1 Rail-to-Rail Input

The MCP6021/2/3/4 amplifier family is designed to not exhibit phase inversion when the input pins exceed the supply voltages. Figure 2-27 shows an input voltage exceeding both supplies with no resulting phase inversion.

The input stage of the MCP6021/2/3/4 family of devices uses two differential input stages in parallel; one operates at low common-mode input voltage ($V_{CM}$), while the other operates at high $V_{CM}$. With this topology, the device operates with $V_{CM}$ up to 0.3V past either supply rail ($V_{SS}$ - 0.3V to $V_{DD}$ + 0.3V) at 25°C. The amplifier input behaves linearly as long as $V_{CM}$ is kept within the specified $V_{CMR}$ limits. The input offset voltage is measured at both $V_{CM} = V_{SS}$ - 0.3V and $V_{DD}$ + 0.3V to ensure proper operation.

Input voltages that exceed the input voltage range ($V_{CMR}$) can cause excessive current to flow in or out of the input pins. Current beyond ±2 mA introduces possible reliability problems. Thus, applications that exceed this rating must externally limit the input current with an input resistor ($R_{IN}$), as shown in Figure 3-1.

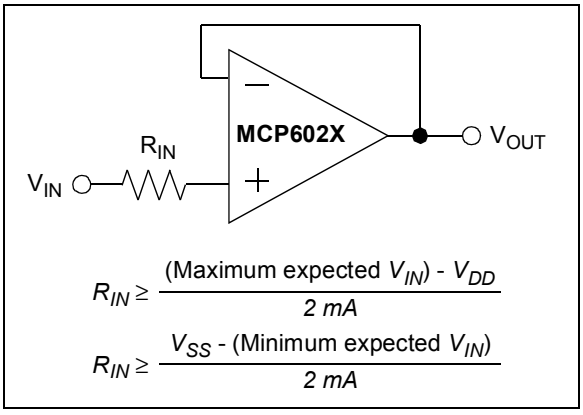



***FIGURE 3-1:*** *$R_{IN}$ limits the current flow into an input pin.*

### 3.2 Rail-to-Rail Output

The Maximum Output Voltage Swing is the maximum swing possible under a particular output load. According to the specification table, the output can reach within 20 mV of either supply rail when $R_L$ = 10 kΩ. See Figure 2-31 and Figure 2-34 for more information concerning typical performance.

### 3.3 MCP6023 Chip Select ($\overline{CS}$)

The MCP6023 is a single amplifier with chip select ($\overline{CS}$). When $\overline{CS}$ is high, the supply current is less than 10 nA (typ) and travels from the $\overline{CS}$ pin to $V_{SS}$, with the amplifier output being put into a high-impedance state. When $\overline{CS}$ is low, the amplifier is enabled. If $\overline{CS}$ is left floating, the amplifier will not operate properly. Figure 1-1 and Figure 2-39 show the output voltage and supply current response to a $\overline{CS}$ pulse.

### 3.4 MCP6021 and MCP6023 Reference Voltage

The single op amps (MCP6021 and MCP6023) have an internal mid-supply reference voltage connected to the $V_{REF}$ pin (see Figure 3-2). The MCP6021 has $\overline{CS}$ internally tied to $V_{SS}$, which always keeps the op amp on and always provides a mid-supply reference. With the MCP6023, taking the $\overline{CS}$ pin high conserves power by shutting down both the op amp and the $V_{REF}$ circuitry. Taking the $\overline{CS}$ pin low turns on the op amp and $V_{REF}$ circuitry.

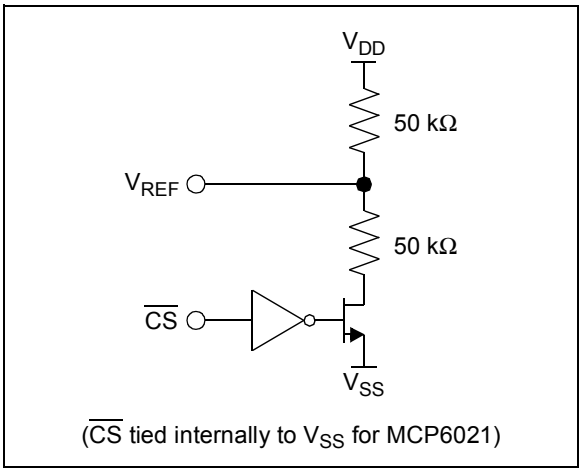



***FIGURE 3-2:*** *Simplified internal $V_{REF}$ circuit (MCP6021 and MCP6023 only).*

See Figure 3-3 for a non-inverting gain circuit using the internal mid-supply reference. The DC-blocking capacitor ($C_B$) also reduces noise by coupling the op amp input to the source.

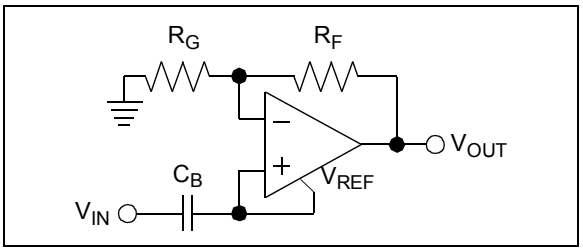



***FIGURE 3-3:*** *Non-inverting gain circuit using $V_{REF}$ (MCP6021 and MCP6023 only).*

To use the internal mid-supply reference for an inverting gain circuit, connect the $V_{REF}$ pin to the non-inverting input, as shown in Figure 3-4. The capacitor $C_B$ helps reduce power supply noise on the output.

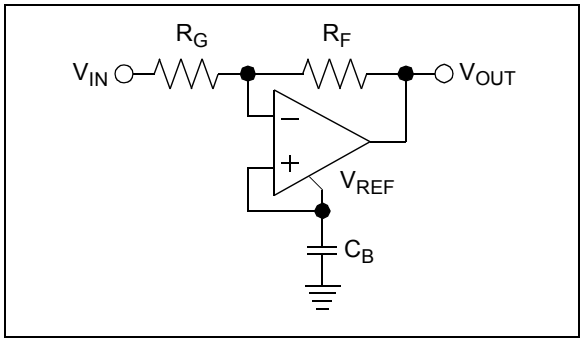



***FIGURE 3-4:*** *Inverting gain circuit using $V_{REF}$ (MCP6021 and MCP6023 only).*

If you don't need the mid-supply reference, leave the $V_{REF}$ pin open.

## 3.5 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases, and the closed loop bandwidth is reduced. This produces gain-peaking in the frequency response, with overshoot and ringing in the step response.

When driving large capacitive loads with these op amps (e.g., > 60 pF when G = +1), a small series resistor at the output ($R_{ISO}$ in Figure 3-5) improves the feedback loop's phase margin (stability) by making the load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

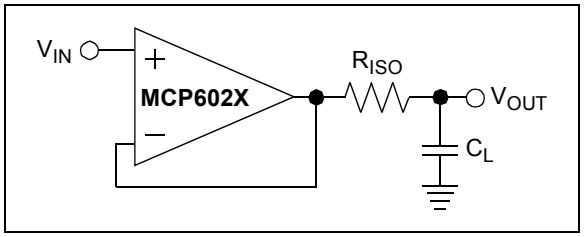



***FIGURE 3-5:*** *Output resistor $R_{ISO}$ stabilizes large capacitive loads.*

Figure 3-6 gives recommended $R_{ISO}$ values for different capacitive laods and gains. The x-axis is the normalized load capacitance ($C_L/G_N$), where $G_N$ is the circuit's noise gain. For non-inverting gains, $G_N$ and the gain are equal. For inverting gains, $G_N$ is 1+|Gain| (e.g., -1 V/V gives $G_N$ = +2 V/V).

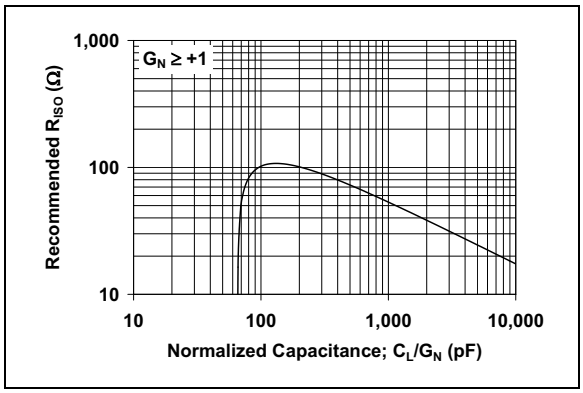



***FIGURE 3-6:*** *Recommended $R_{ISO}$ values for capacitive loads.*

After selecting $R_{ISO}$ for your circuit, double-check the resulting frequency response peaking and step response overshoot. Evaluation on the bench and simulations with the MCP6021/2/3/4 Spice macro model are very helpful. Modify $R_{ISO}$'s value until the response is reasonable.

## 3.6 Supply Bypass

With this family of operational amplifiers, the power supply pin ($V_{DD}$ for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good, high-frequency performance. It also needs a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with other parts.

## 3.7 PCB Surface Leakage

In applications where low input bias current is critical, PCB (printed circuit board) surface-leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow, which is greater than the MCP6021/2/3/4 family's bias current at 25°C (1 pA, typ).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 3-7.

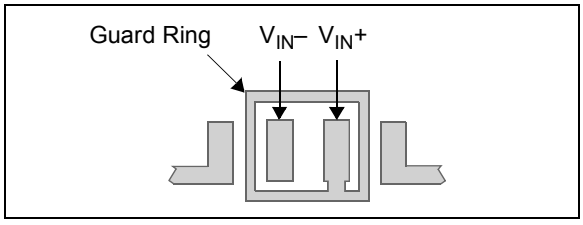



***FIGURE 3-7:*** *Example guard ring layout.*

1. Inverting (Figure 3-7) and Transimpedance Gain Amplifiers (convert current to voltage, such as photo detectors).
   a. Connect the guard ring to the non-inverting input pin ($V_{IN}$+). This biases the guard ring to the same reference voltage as the op amp's input (e.g., $V_{DD}$/2 or ground).
   b. Connect the inverting pin ($V_{IN}$–) to the input with a wire that does not touch the PCB surface.
2. Non-inverting Gain and Unity-Gain Buffer
   a. Connect the guard ring to the inverting input pin ($V_{IN}$–); this biases the guard ring to the common mode input voltage.
   b. Connect the non-inverting pin ($V_{IN}$+) to the input with a wire that does not touch the PCB surface.

## 3.8 High-Speed PCB Layout

Due to their speed capabilities, a little extra care in the PCB (Printed Circuit Board) layout can make a significant difference in the performance of these op amps. Good PC board layout techniques will help you achieve the performance shown in the Electrical Characteristics and Typical Performance Curves, while also helping you minimize EMC (Electro-Magnetic Compatibility) issues.

Use a solid ground plane and connect the bypass local capacitor(s) to this plane with minimal length traces. This cuts down inductive and capacitive crosstalk.

Separate digital from analog, low-speed from high-speed and low power from high power. This will reduce interference.

Keep sensitive traces short and straight. Separating them from interfering components and traces. This is especially important for high-frequency (low rise-time) signals.

Sometimes it helps to place guard traces next to victim traces. They should be on both sides of the victim trace, and as close as possible. Connect the guard trace to ground plane at both ends, and in the middle for long traces.

Use coax cables (or low inductance wiring) to route signal and power to and from the PCB.

## 3.9 Typical Applications

### 3.9.1 A/D CONVERTER DRIVER AND ANTI-ALIASING FILTER

Figure 3-8 shows a third-order Butterworth filter that can be used as an A/D converter driver. It has a bandwidth of 20 kHz and a reasonable step response. It will work well for conversion rates of 80 ksps and greater (it has 29 dB attenuation at 60 kHz).

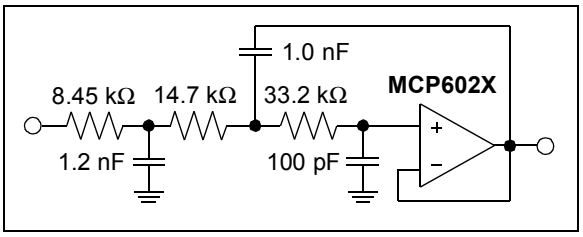



***FIGURE 3-8:*** *A/D converter driver and anti-aliasing filter with a 20 kHz cutoff frequency.*

This filter can easily be adjusted to another bandwidth by multiplying all capacitors by the same factor. Alternatively, the resistors can all be scaled by another common factor to adjust the bandwidth.

### 3.9.2 OPTICAL DETECTOR AMPLIFIER

Figure 3-9 shows the MCP6021 op amp used as a transimpedance amplifier in a photo detector circuit. The photo detector looks like a capacitive current source, so the 100 kΩ resistor gains the input signal to a reasonable level. The 5.6 pF capacitor stabilizes this circuit and produces a flat frequency response with a bandwidth of 370 kHz.

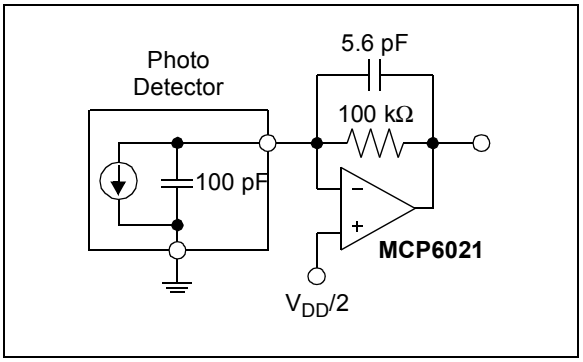



***FIGURE 3-9:*** *Transimpedance amplifier for an optical detector.*

## 4.0 DESIGN TOOLS

Microchip provides the basic design tools needed for the MCP6021/2/3/4 family of op amps.

### 4.1 SPICE Macro Model

The latest SPICE macro model for the MCP6021/2/3/4 op amps is available on our web site (www.microchip.com). This model is intended as an initial design tool that works well in the op amp's linear region of operation at room temperature. See the model file for information on its capabilities.

Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specs and plots.

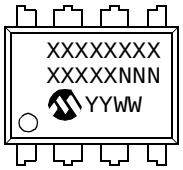
### 4.2 FilterLab® Software

The FilterLab® software is an innovative tool that simplifies analog active filter (using op amps) design. Available at no cost from our web site (at www.microchip.com), the FilterLab software active filter design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the Macro Model to simulate actual filter performance.

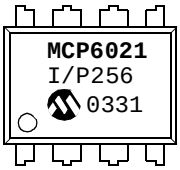
## 5.0 PACKAGING INFORMATION

### 5.1 Package Marking Information

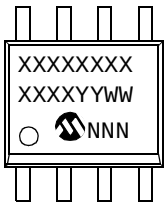
8-Lead PDIP (300 mil)



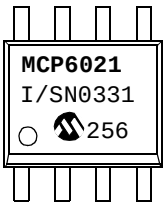

Example:



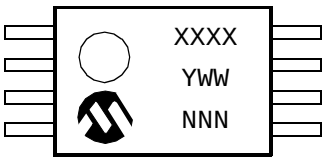

8-Lead SOIC (150 mil)



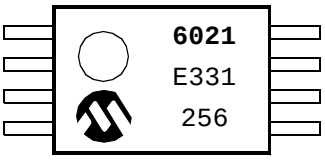

Example:




8-Lead TSSOP




Example:



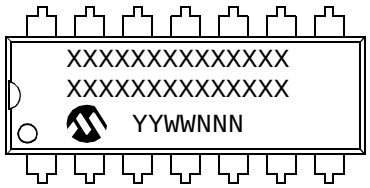

| | | |
|---|---|---|
| **Legend:** | XX...X | Customer specific information* |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

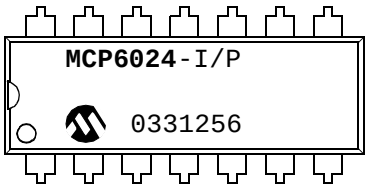
***** Standard device marking consists of Microchip part number, year code, week code, and traceability code.

## Package Marking Information (Continued)

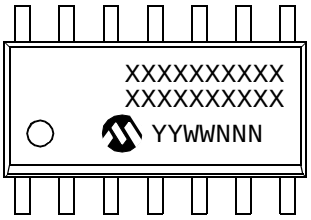
14-Lead PDIP (300 mil) **(MCP6024)**



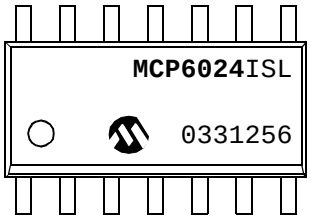

Example:



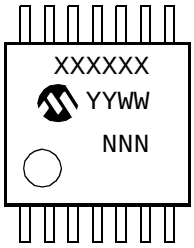

14-Lead SOIC (150 mil) **(MCP6024)**



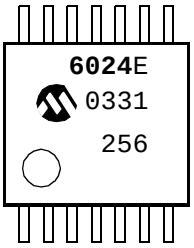

Example:



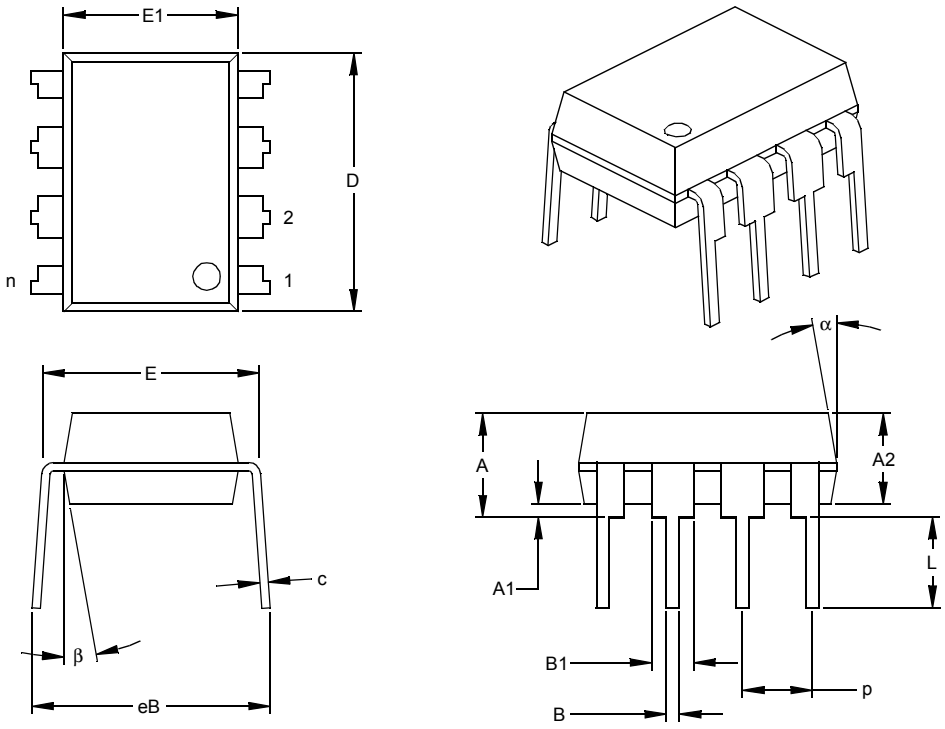

14-Lead TSSOP **(MCP6024)**




Example:



## 8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

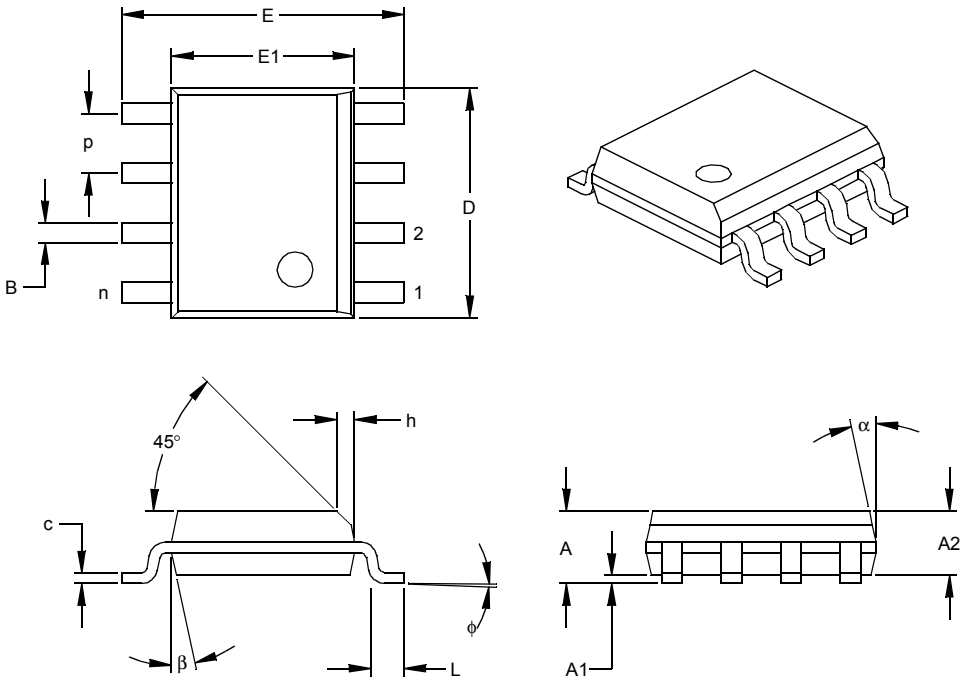



| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 8 | | | 8 | |
| Pitch | p | | .100 | | | 2.54 | |
| Top to Seating Plane | A | .140 | .155 | .170 | 3.56 | 3.94 | 4.32 |
| Molded Package Thickness | A2 | .115 | .130 | .145 | 2.92 | 3.30 | 3.68 |
| Base to Seating Plane | A1 | .015 | | | 0.38 | | |
| Shoulder to Shoulder Width | E | .300 | .313 | .325 | 7.62 | 7.94 | 8.26 |
| Molded Package Width | E1 | .240 | .250 | .260 | 6.10 | 6.35 | 6.60 |
| Overall Length | D | .360 | .373 | .385 | 9.14 | 9.46 | 9.78 |
| Tip to Seating Plane | L | .125 | .130 | .135 | 3.18 | 3.30 | 3.43 |
| Lead Thickness | c | .008 | .012 | .015 | 0.20 | 0.29 | 0.38 |
| Upper Lead Width | B1 | .045 | .058 | .070 | 1.14 | 1.46 | 1.78 |
| Lower Lead Width | B | .014 | .018 | .022 | 0.36 | 0.46 | 0.56 |
| Overall Row Spacing § | eB | .310 | .370 | .430 | 7.87 | 9.40 | 10.92 |
| Mold Draft Angle Top | α | 5 | 10 | 15 | 5 | 10 | 15 |
| Mold Draft Angle Bottom | β | 5 | 10 | 15 | 5 | 10 | 15 |

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

## 8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)

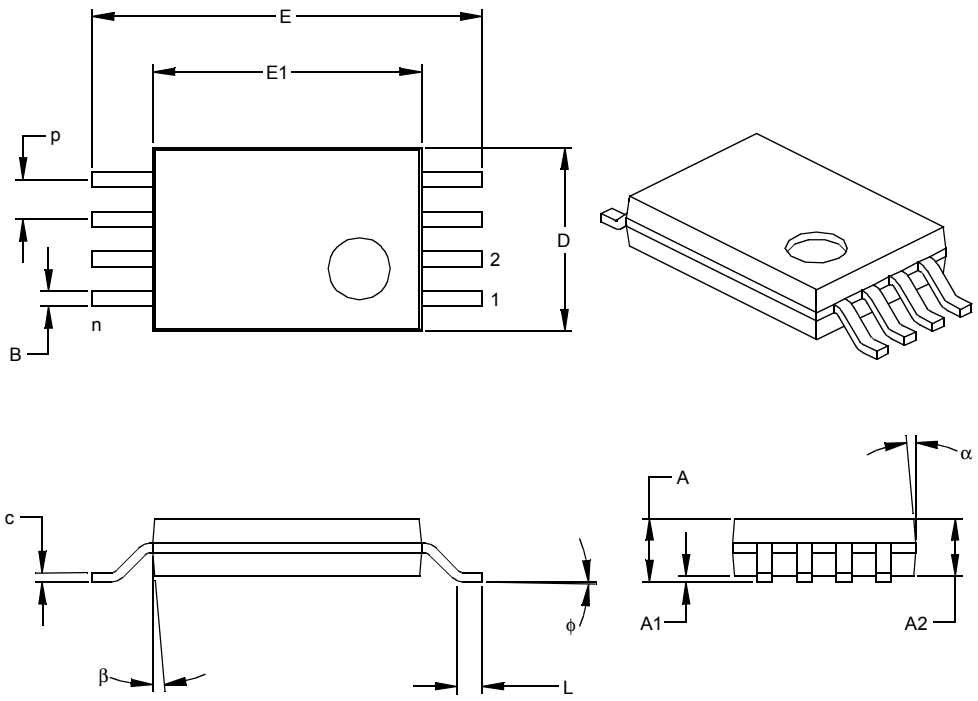



| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 8 | | | 8 | |
| Pitch | p | | .050 | | | 1.27 | |
| Overall Height | A | .053 | .061 | .069 | 1.35 | 1.55 | 1.75 |
| Molded Package Thickness | A2 | .052 | .056 | .061 | 1.32 | 1.42 | 1.55 |
| Standoff § | A1 | .004 | .007 | .010 | 0.10 | 0.18 | 0.25 |
| Overall Width | E | .228 | .237 | .244 | 5.79 | 6.02 | 6.20 |
| Molded Package Width | E1 | .146 | .154 | .157 | 3.71 | 3.91 | 3.99 |
| Overall Length | D | .189 | .193 | .197 | 4.80 | 4.90 | 5.00 |
| Chamfer Distance | h | .010 | .015 | .020 | 0.25 | 0.38 | 0.51 |
| Foot Length | L | .019 | .025 | .030 | 0.48 | 0.62 | 0.76 |
| Foot Angle | φ | 0 | 4 | 8 | 0 | 4 | 8 |
| Lead Thickness | c | .008 | .009 | .010 | 0.20 | 0.23 | 0.25 |
| Lead Width | B | .013 | .017 | .020 | 0.33 | 0.42 | 0.51 |
| Mold Draft Angle Top | α | 0 | 12 | 15 | 0 | 12 | 15 |
| Mold Draft Angle Bottom | β | 0 | 12 | 15 | 0 | 12 | 15 |

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

## 8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)

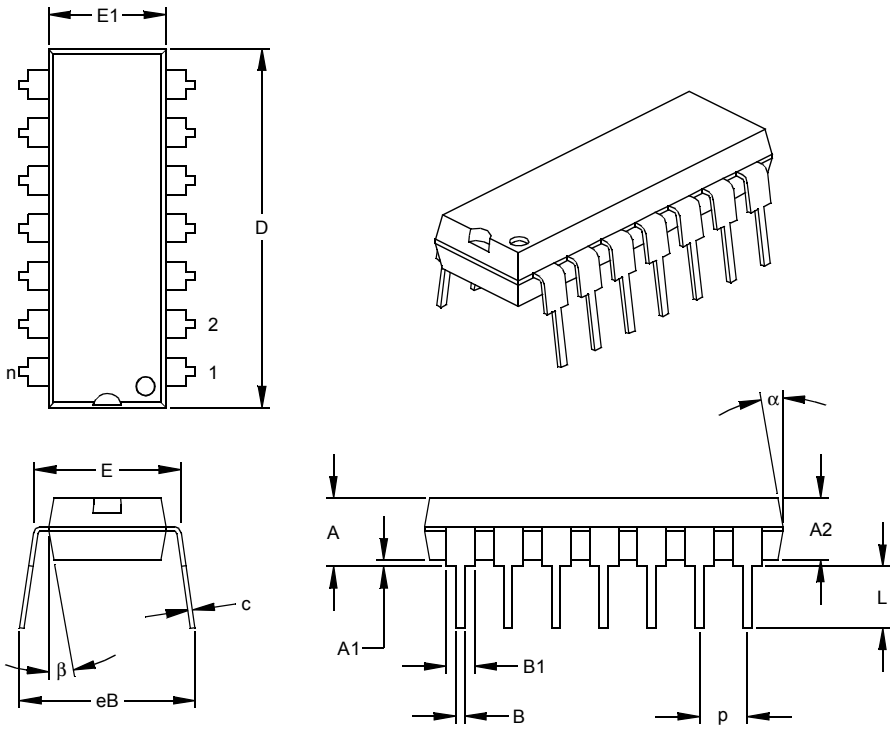



| Units | | INCHES | | | MILLIMETERS* | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 8 | | | 8 | |
| Pitch | p | | .026 | | | 0.65 | |
| Overall Height | A | | | .043 | | | 1.10 |
| Molded Package Thickness | A2 | .033 | .035 | .037 | 0.85 | 0.90 | 0.95 |
| Standoff § | A1 | .002 | .004 | .006 | 0.05 | 0.10 | 0.15 |
| Overall Width | E | .246 | .251 | .256 | 6.25 | 6.38 | 6.50 |
| Molded Package Width | E1 | .169 | .173 | .177 | 4.30 | 4.40 | 4.50 |
| Molded Package Length | D | .114 | .118 | .122 | 2.90 | 3.00 | 3.10 |
| Foot Length | L | .020 | .024 | .028 | 0.50 | 0.60 | 0.70 |
| Foot Angle | φ | 0 | 4 | 8 | 0 | 4 | 8 |
| Lead Thickness | c | .004 | .006 | .008 | 0.09 | 0.15 | 0.20 |
| Lead Width | B | .007 | .010 | .012 | 0.19 | 0.25 | 0.30 |
| Mold Draft Angle Top | α | 0 | 5 | 10 | 0 | 5 | 10 |
| Mold Draft Angle Bottom | β | 0 | 5 | 10 | 0 | 5 | 10 |

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005” (0.127mm) per side.
JEDEC Equivalent: MO-153
Drawing No. C04-086

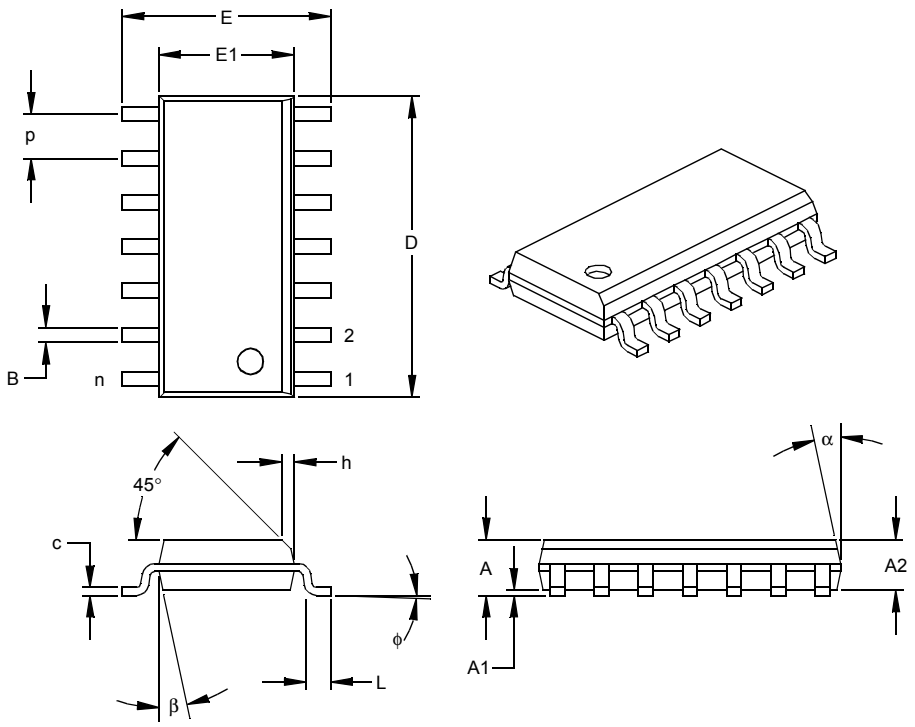
## 14-Lead Plastic Dual In-line (P) – 300 mil (PDIP)




| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 14 | | | 14 | |
| Pitch | p | | .100 | | | 2.54 | |
| Top to Seating Plane | A | .140 | .155 | .170 | 3.56 | 3.94 | 4.32 |
| Molded Package Thickness | A2 | .115 | .130 | .145 | 2.92 | 3.30 | 3.68 |
| Base to Seating Plane | A1 | .015 | | | 0.38 | | |
| Shoulder to Shoulder Width | E | .300 | .313 | .325 | 7.62 | 7.94 | 8.26 |
| Molded Package Width | E1 | .240 | .250 | .260 | 6.10 | 6.35 | 6.60 |
| Overall Length | D | .740 | .750 | .760 | 18.80 | 19.05 | 19.30 |
| Tip to Seating Plane | L | .125 | .130 | .135 | 3.18 | 3.30 | 3.43 |
| Lead Thickness | c | .008 | .012 | .015 | 0.20 | 0.29 | 0.38 |
| Upper Lead Width | B1 | .045 | .058 | .070 | 1.14 | 1.46 | 1.78 |
| Lower Lead Width | B | .014 | .018 | .022 | 0.36 | 0.46 | 0.56 |
| Overall Row Spacing § | eB | .310 | .370 | .430 | 7.87 | 9.40 | 10.92 |
| Mold Draft Angle Top | α | 5 | 10 | 15 | 5 | 10 | 15 |
| Mold Draft Angle Bottom | β | 5 | 10 | 15 | 5 | 10 | 15 |

* Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-005

### 14-Lead Plastic Small Outline (SL) – Narrow, 150 mil (SOIC)

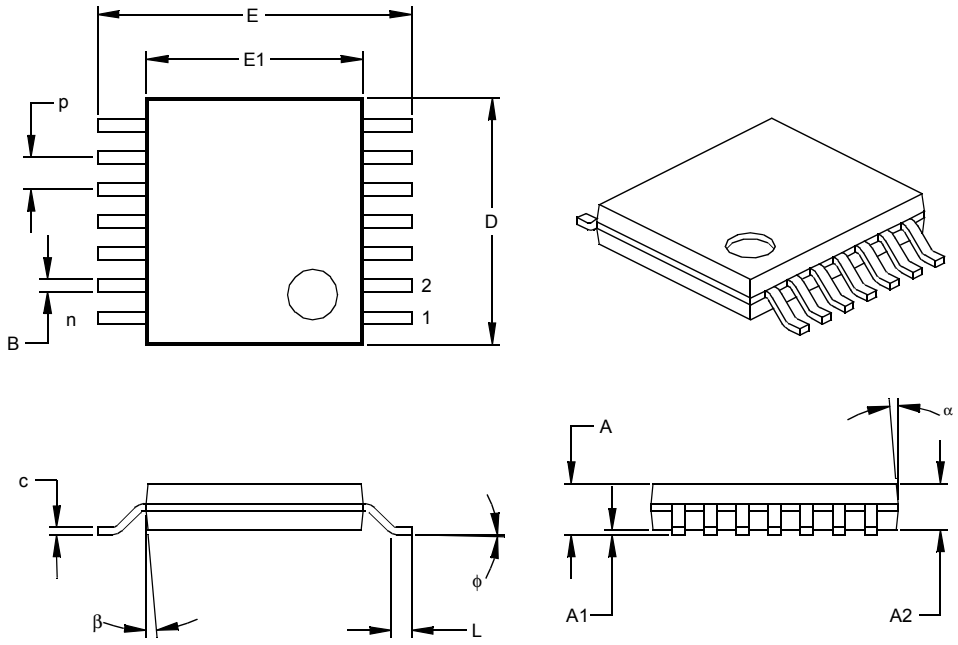



| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 14 | | | 14 | |
| Pitch | p | | .050 | | | 1.27 | |
| Overall Height | A | .053 | .061 | .069 | 1.35 | 1.55 | 1.75 |
| Molded Package Thickness | A2 | .052 | .056 | .061 | 1.32 | 1.42 | 1.55 |
| Standoff § | A1 | .004 | .007 | .010 | 0.10 | 0.18 | 0.25 |
| Overall Width | E | .228 | .236 | .244 | 5.79 | 5.99 | 6.20 |
| Molded Package Width | E1 | .150 | .154 | .157 | 3.81 | 3.90 | 3.99 |
| Overall Length | D | .337 | .342 | .347 | 8.56 | 8.69 | 8.81 |
| Chamfer Distance | h | .010 | .015 | .020 | 0.25 | 0.38 | 0.51 |
| Foot Length | L | .016 | .033 | .050 | 0.41 | 0.84 | 1.27 |
| Foot Angle | φ | 0 | 4 | 8 | 0 | 4 | 8 |
| Lead Thickness | c | .008 | .009 | .010 | 0.20 | 0.23 | 0.25 |
| Lead Width | B | .014 | .017 | .020 | 0.36 | 0.42 | 0.51 |
| Mold Draft Angle Top | α | 0 | 12 | 15 | 0 | 12 | 15 |
| Mold Draft Angle Bottom | β | 0 | 12 | 15 | 0 | 12 | 15 |

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-065

## 14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)




| Units | | INCHES | | | MILLIMETERS* | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 14 | | | 14 | |
| Pitch | p | | .026 | | | 0.65 | |
| Overall Height | A | | | .043 | | | 1.10 |
| Molded Package Thickness | A2 | .033 | .035 | .037 | 0.85 | 0.90 | 0.95 |
| Standoff § | A1 | .002 | .004 | .006 | 0.05 | 0.10 | 0.15 |
| Overall Width | E | .246 | .251 | .256 | 6.25 | 6.38 | 6.50 |
| Molded Package Width | E1 | .169 | .173 | .177 | 4.30 | 4.40 | 4.50 |
| Molded Package Length | D | .193 | .197 | .201 | 4.90 | 5.00 | 5.10 |
| Foot Length | L | .020 | .024 | .028 | 0.50 | 0.60 | 0.70 |
| Foot Angle | φ | 0 | 4 | 8 | 0 | 4 | 8 |
| Lead Thickness | c | .004 | .006 | .008 | 0.09 | 0.15 | 0.20 |
| Lead Width | B | .007 | .010 | .012 | 0.19 | 0.25 | 0.30 |
| Mold Draft Angle Top | α | 0 | 5 | 10 | 0 | 5 | 10 |
| Mold Draft Angle Bottom | β | 0 | 5 | 10 | 0 | 5 | 10 |

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005” (0.127mm) per side.
JEDEC Equivalent: MO-153
Drawing No. C04-087

**NOTES:**

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | X | /XX |
|---|---|---|
| Device | Temperature Range | Package |

| | | |
|---|---|---|
| Device: | MCP6021 | CMOS Single Op Amp |
| | MCP6021T | CMOS Single Op Amp (Tape and Reel for SOIC, TSSOP) |
| | MCP6022 | CMOS Dual Op Amp |
| | MCP6022T | CMOS Dual Op Amp (Tape and Reel for SOIC and TSSOP) |
| | MCP6023 | CMOS Single Op Amp w/ $\overline{CS}$ Function |
| | MCP6023T | CMOS Single Op Amp w/ $\overline{CS}$ Function (Tape and Reel for SOIC and TSSOP) |
| | MCP6024 | CMOS Quad Op Amp |
| | MCP6024T | CMOS Quad Op Amp (Tape and Reel for SOIC and TSSOP) |
| Temperature Range: | I = | -40°C to +85°C |
| | E = | -40×C to +125×C |
| Package: | P = | Plastic DIP (300 mil Body), 8-lead, 14-lead |
| | SN = | Plastic SOIC (150mil Body), 8-lead |
| | SL = | Plastic SOIC (150 mil Body), 14-lead |
| | ST = | Plastic TSSOP, 8-lead, 14-lead |

**Examples:**

| | | |
|---|---|---|
| a) | MCP6021-I/P: | Industrial temperature, PDIP package. |
| b) | MCP6021-E/P: | Extended temperature, PDIP package. |
| c) | MCP6021-E/SN: | Extended temperature, SOIC package. |
| a) | MCP6022-I/P: | Industrial temperature, PDIP package. |
| b) | MCP6022-E/P: | Extended temperature, PDIP package. |
| c) | MCP6022T-E/ST: | Tape and Reel, Extended temperature, TSSOP package. |
| a) | MCP6023-I/P: | Industrial temperature, PDIP package. |
| b) | MCP6023-E/P: | Extended temperature, PDIP package. |
| c) | MCP6023-E/SN: | Extended temperature, SOIC package. |
| a) | MCP6024-I/SL: | Industrial temperature, SOIC package. |
| b) | MCP6024-E/SL: | Extended temperature, SOIC package. |
| c) | MCP6024T-E/ST: | Tape and Reel, Extended temperature, TSSOP package. |

## Sales and Support

**Data Sheets**
Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

**Customer Notification System**
Register on our web site (www.microchip.com/cn) to receive the most current information on our products.

**NOTES:**

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.



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*Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999 and Mountain View, California in March 2002. The Company's quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, non-volatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001 certified.*

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**Toronto**
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Fax: 61-2-9868-6755

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Fuzhou 350001, China
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Fax: 86-591-7503521

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