# BD9897FS



STRUCTURE Silicon Monolithic Integrated Circuit

NAME OF PRODUCT DC-AC Inverter Control IC

TYPE **BD9897FS**

FUNCTION
- 36V High voltage process
- 1ch control with Full-Bridge
- Lamp current and voltage sense feed back control
- Sequencing easily achieved with Soft Start Control
- Short circuit protection with Timer Latch
- Under Voltage Lock Out
- Mode-selectable the operating or stand-by mode by stand-by pin
- Synchronous operating the other BD9897FS IC's
- BURST mode controlled by PWM and DC input
- Output liner Control by external DC voltage

## ○Absolute Maximum Ratings (Ta = 25℃)

| Parameter | Symbol | Limits | Unit |
|---|---|---|---|
| Supply Voltage | Vcc | 36 | V |
| BST pin | BST | 40 | V |
| SW pin | SW | 36 | V |
| BST-SW voltage difference | BST-SW | 7 | V |
| Operating Temperature Range | Topr | -40～+85 | ℃ |
| Storage Temperature Range | Tstg | -55～+150 | ℃ |
| Maximum Junction Temperature | Tjmax | +150 | ℃ |
| Power Dissipation | Pd | 950* | mW |

*Pd derate at 7.6mW/℃ for temperature above Ta = 25℃ (When mounted on a PCB 70.0mm×70.0mm×1.6mm)

## ○Operating condition

| Parameter | Symbol | Limits | Unit |
|---|---|---|---|
| Supply voltage | Vcc | 7.5～30.0 | V |
| BST voltage | BST | 4.0～36.0 | V |
| BST-SW voltage difference | BST-SW | 4.0～6.5 | V |
| CT oscillation frequency | fCT | 60～180 | kHz |
| BCT oscillation frequency | fBCT | 0.05～1.00 | kHz |

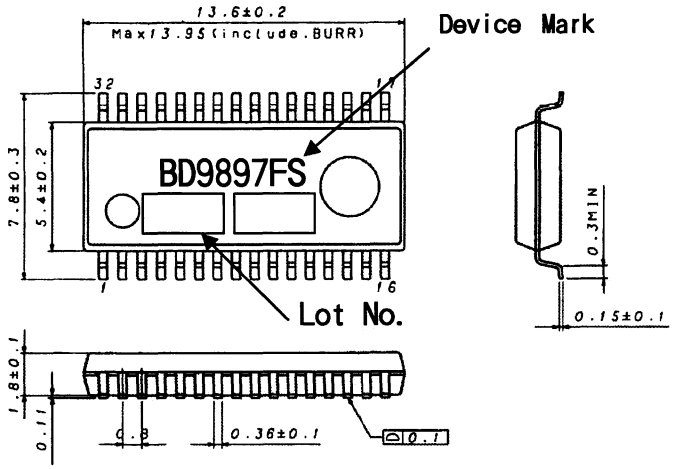
Status of this document
The Japanese version of this document is the official specification.
Please use the translation version of this document as a reference to expedite understanding of the official version.
If these are any uncertainty in translation version of this document, official version takes priority.

○ Electric Characteristics (Ta=25℃, VCC=24V)

| Parameter | Symbol | Limits | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | | |
| ((WHOLE DEVICE)) | | | | | | |
| Operating current | Icc1 | — | 7.2 | 13 | mA | CT_SYNC_IN = OPEN |
| Stand-by current | Icc2 | — | 13.0 | 30.0 | μA | |
| ((STAND BY CONTROL)) | | | | | | |
| Stand-by voltage H | VstH | 2.0 | — | VCC | V | System O N |
| Stand-by voltage L | VstL | -0.3 | — | 0.8 | V | System O F F |
| ((UVLO BLOCK))) | | | | | | |
| Operating voltage (VCC) | VuvloH | 5.7 | 6.0 | 6.3 | V | |
| Hesteresis width (VCC) | ⊿VCC_Vuvlo | 0.26 | 0.35 | 0.43 | V | |
| Operating voltage (UVLO) | Vuvlo2 | 2.179 | 2.25 | 2.321 | V | |
| Hesteresis width (UVLO) | ⊿Vuvlo | 0.074 | 0.098 | 0.122 | V | |
| ((REG BLOCK)) | | | | | | |
| REG output voltage | VREG | 5.68 | 5.80 | 5.92 | V | VCC>7.0V |
| REG source current | IREG | 20.0 | — | — | mA | |
| ((OSC BLOCK)) | | | | | | |
| Active edge setting current | Iact | 1.35/(RT*7) | 1.5/(RT*6) | 1.65/(RT*5) | A | |
| Negative edge setting current | Ineg | Iact×29 | Iact×35 | Iact×41 | A | |
| OSC Max voltage | VOSCH | 1.8 | 2.0 | 2.2 | V | fCT=120kHz |
| OSC Min voltage | VOSCL | 0.35 | 0.45 | 0.60 | V | fCT=120kHz |
| Soft start current | ISS | 0.6 | 1.1 | 1.6 | μA | |
| SRT ON resistance | RSRT | — | 100 | 200 | Ω | |
| ((BOSC BLOCK)) | | | | | | |
| BOSC Max voltage | VBCTH | 1.94 | 2.00 | 2.06 | V | fBCT=0.3kHz |
| BOSC Min voltage | VBCTL | 0.40 | 0.50 | 0.60 | V | fBCT=0.3kHz |
| BOSC constant current | IBCT | 1.35/BRT | 1.5/RT | 1.65/RT | A | VBCT=0.2V |
| BOSC frequency | fBCT | 291 | 300 | 309 | Hz | (BRT=33kΩ BCT=0.048μF) |
| ((FEED BACK BLOCK)) | | | | | | |
| IS threshold voltage 1 | VIS① | 1.225 | 1.250 | 1.275 | V | |
| IS threshold voltage 2 | VIS② | — | VREFIN | VIS① | V | VREF applying voltage |
| VS threshold voltage | VVS | 1.220 | 1.250 | 1.280 | V | |
| IS source current 1 | IIS1 | — | — | 0.9 | μA | DUTY=2.2V |
| IS source current 2 | IIS2 | 32 | 50 | 68 | μA | DUTY=0V IS=0.5V |
| VS source current | IVS | — | — | 0.9 | μA | |
| IS COMP detect voltage ① | VISCOMP① | 0.90 | 0.94 | 0.98 | V | VREFIN≧1.25V |
| IS COMP detect voltage ② | VISCOMP② | — | VREFIN×0.73 | — | V | VREFIN<1.25V |
| VREF input voltage range | VREFIN | 0.6 | — | 1.6 | V | No effect at VREF>1.25V |
| ((DUTY BLOCK)) | | | | | | |
| High voltage | VDUTY-OUTH | 2.8 | 3.1 | 3.4 | V | |
| Low voltage | VDUTY-OUTL | — | - | 0.5 | V | |
| DUTY-OUT sink resistance | RDUTY-OUTSink | — | 150 | 300 | Ω | |
| DUTY-OUT source resistance | RDUTY-OUTSouce | — | 250 | 500 | Ω | |
| ((OUTPUT BLOCK)) | | | | | | |
| LN output sink resistance | RsinkLN | — | 1.5 | 3.0 | Ω | |
| LN output source resistance | RsourceLN | — | 5 | 10 | Ω | |
| HN output sink resistance | RsinkHN | — | 2.5 | 5.0 | Ω | VBST-VSW=5.0V |
| HN output source resistance | RsourceLN | — | 5 | 10 | Ω | VBST-VSW=5.0V |
| MAX DUTY | MAX DUTY | 46.0 | 48.0 | 49.5 | % | FOUT=60kHz |
| OFF period | TOFF | 100 | 200 | 400 | ns | |
| Drive output frequency | FOUT | 58.5 | 60.0 | 61.5 | kHz | (RT=4.7kΩ CT=235pF) |
| ((TIMER LATCH BLOCK)) | | | | | | |
| Timer Latch setting voltage | VCP | 1.94 | 2.0 | 2.06 | V | |
| Timer Latch setting current | ICP | 0.40 | 0.55 | 0.70 | μA | |
| ((COMP CLOCK)) | | | | | | |
| COMP1 over voltage detect voltage | VCOMPH | 2.460 | 2.485 | 2.510 | V | VSS>2.2V |
| COMP2 over voltage detect voltage | VCOMP2_H | 2.460 | 2.485 | 2.510 | V | VSS>2.2V |
| COMP2 under voltage detect voltage ① | VCOMP_L_1 | 1.225 | 1.25 | 1.275 | V | VSS>2.2V |
| COMP2 under voltage detect voltage ② | VCOMP_L_2 | 0.606 | 0.625 | 0.644 | V | VSS<2.2V |
| ((Synchronous Block)) | | | | | | |
| High voltage | VCT_SYNCH | 2.8 | 3.1 | 3.4 | V | |
| Low voltage | VCT_SYNCL | — | — | 0.5 | V | |
| CT_SYNC sink resistance | RCT_SYNC_SYNC | — | 150 | 300 | Ω | |
| CT_SYNC source resistance | RCT_SYNC_SOURCE | — | 370 | 740 | Ω | |
| High voltage input range | VCT_SYNC_IN_H | 2.0 | — | 3.3 | V | |
| Low voltage input range | VCT_SINK_IN_L | -0.3 | — | 0.6 | V | |

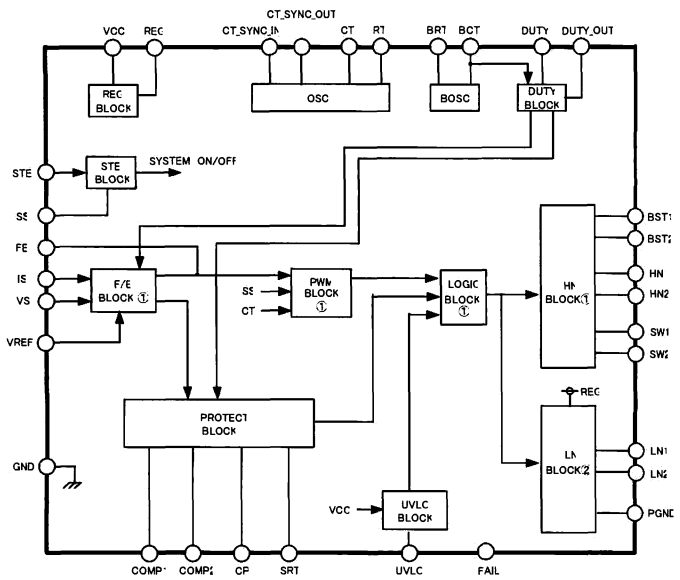
(This product is not designed to be radiation-resistant.)

## ○Package Dimensions




SSOP-A32 (Unit : mm)

## ○Block Diagram




## ○Pin Description

| PIN No. | PIN NAME | FUNCTION |
|---|---|---|
| 1 | PGND | Ground for FET drivers |
| 2 | LN2 | NMOS FET driver |
| 3 | HN2 | NMOS FET driver |
| 4 | SW2 | Lower rail voltage for HN2 output |
| 5 | BST2 | Boot-Strap input for HN2 output |
| 6 | CT_SYNC_IN | CT synchronous signal input pin |
| 7 | CT_SYNC_OUT | CT synchronous signal output pin |
| 8 | SRT | External resistor from SRT to RT for adjusting the triangle oscillator |
| 9 | RT | External resistor from SRT to RT for adjusting the triangle oscillator |
| 10 | CT | External capacitor from CT to GND for adjusting the triangle oscillator |
| 11 | GND | GROUND |
| 12 | BCT | External capacitor from BCT to GND for adjusting the BURST triangle oscillator |
| 13 | BRT | External resistor from BRT to GND for adjusting the BURST triangle oscillator |
| 14 | DUTY | Control PWM mode and BURST mode |
| 15 | DUTY_OUT | BURST signal output pin |
| 16 | STB | Stand-by switch |
| 17 | CP | External capacitor from CP to GND for Timer Latch |
| 18 | FAIL | COMP2 under voltage protect clock output |
| 19 | VREF | Reference voltage input pin for Error amplifier |
| 20 | VS | Error amplifier input |
| 21 | IS | Error amplifier input |
| 22 | FB | Error amplifier output |
| 23 | SS | External capacitor from SS to GND for Soft Start Control |
| 24 | COMP2 | Under, over voltage detect pin |
| 25 | COMP1 | Over voltage detect pin |
| 26 | VCC | Supply voltage input |
| 27 | UVLO | External Under Voltage Lock Out |
| 28 | REG | Internal regulator output |
| 29 | BST1 | Boot-Strap input for HN1 output |
| 30 | SW1 | Lower rail voltage for HN1 output |
| 31 | HN1 | NMOS FET driver |
| 32 | LN1 | NMOS FET driver |

○NOTE FOR USE

1. When designing the external circuit, including adequate margins for variation between external devices and IC. Use adequate margins for steady state and transient characteristics.
2. The circuit functionality is guaranteed within of ambient temperature operation range as long as it is within recommended operating range. The standard electrical characteristic values cannot be guaranteed at other voltages in the operating ranges, however the variation will be small.
3. Mounting failures, such as misdirection or miscounts, may harm the device.
4. A strong electromagnetic field may cause the IC to malfunction.
5. The GND pin should be the location within ±0.3V compared with the PGND pin.
6. BD9897FS incorporate a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation of the thermal shutdown circuit is assumed.
7. Absolute maximum ratings are those values that, if exceeded, may cause the life of a device to become significantly shortened. Moreover, the exact failure mode caused by short or open is not defined. Physical countermeasures, such as a fuse, need to be considered when using a device beyond its maximum ratings.
8. About the external FET, the parasitic Capacitor may cause the gate voltage to change, when the drain voltage is switching. Make sure to leave adequate margin for this IC variation.
9. On operating Slow Start Control (SS is less than 2.2V), It does not operate Timer Latch.
10. By STB voltage, BD9897FS are changed to 2 states. Therefore, do not input STB pin voltage between one state and the other state (0.8～2.0V).
11. The pin connected a connector need to connect to the resistor for electrical surge destruction.
    This IC is a monolithic IC which (as shown is Fig-1) has $P^+$ substrate and between the various pins. A P-N junction is formed from this P layer of each pin. For example, the relation between each potential is as follows,
    ○(When GND > PinB and GND > PinA, the P-N junction operates as a parasitic diode.)
    ○(When PinB > GND > PinA, the P-N junction operates as a parasitic transistor.)
    Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits as well as operation faults and physical damage. Accordingly you must not use methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin.
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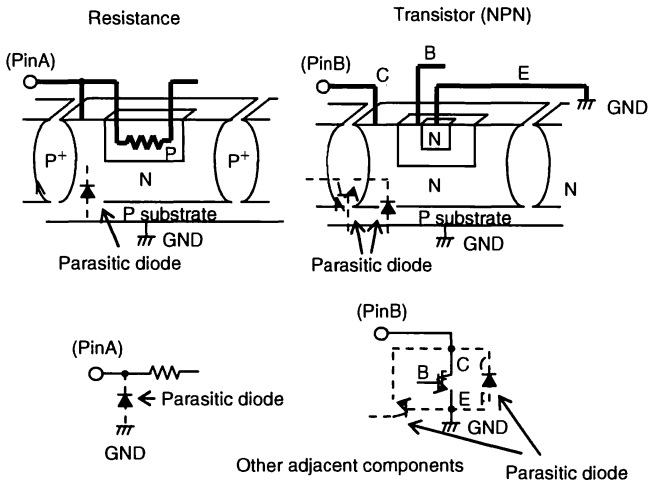


Fig-1 Simplified structure of a Bipolar IC