HD74HC74

Dual D-type Flip-Flops (with Preset and Clear)

HITACHI

Description

The flip-flop has independent data, preset, clear, and clock inputs and Q and $\overline{Q}$ outputs. The logic level present at thte data input is transferred to the output during the positive going transition to the clock pulse. Preset and clear are independent of the clock and accomplished by a low level at the appropriate input.

Features

- High Speed Operation: t_{pd} (Clock to Q or $\overline{Q}$) = 14 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 2 to 6 V
- Low Input Current: 1 µA max
- Low Quiescent Supply Current: I_{CC} (static) = 2 µA max (Ta = 25°C)

Function Table

Inputs				Outputs	
Preset	**Clear**	**Clock**	**Data**	**Q**	**$\overline{Q}$**
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*[1]	H*[1]
H	H	⎍	H	H	L
H	H	⎍	L	L	H
H	H	L	X	no change	no change
H	H	H	X	no change	no change
H	H	⎏	X	no change	no change

Note: 1. Q and $\overline{Q}$ will remain HIGH as long as Preset and Clear are Low, but Q and $\overline{Q}$ are unpredictable, if Preset and Clear go HIGH simultaneously.

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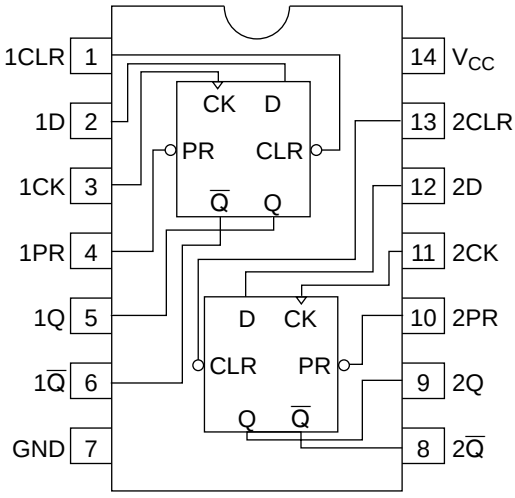
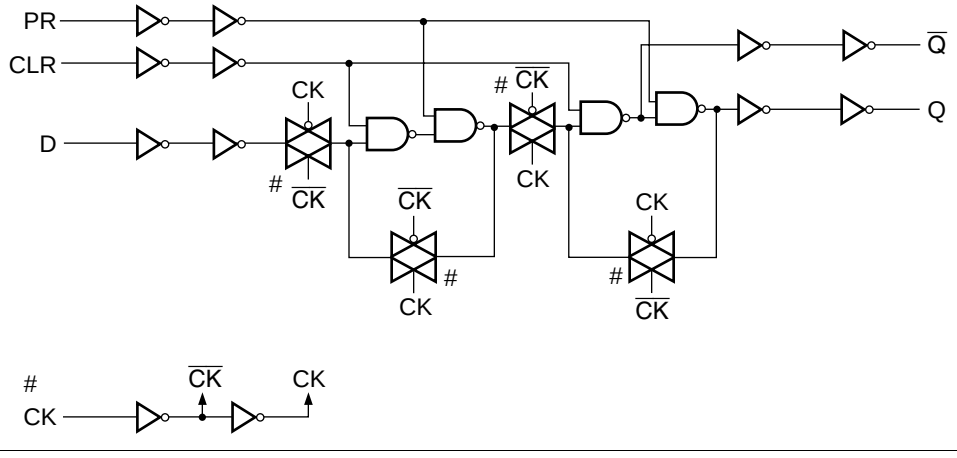
Pin Arrangement



(Top view)

Logic Diagram (1/2)



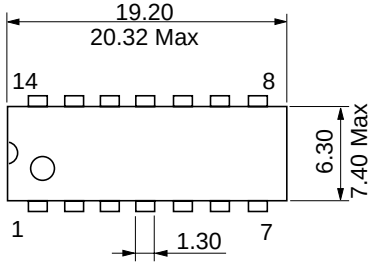
DC Characteristics

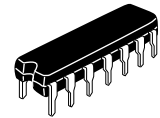
Item	Symbol	V_{CC} (V)	Ta = 25°C Min	Typ	Max	Ta = –40 to +85°C Min	Max	Unit	Test Conditions	
Input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V_{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V_{IH} or V_{IL}	I_{OH} = –20 µA
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I_{OH} = –4 mA
		6.0	5.68	—	—	5.63	—			I_{OH} = –5.2 mA
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V_{IH} or V_{IL}	I_{OL} = 20 µA
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			I_{OL} = 4 mA
		6.0	—	—	0.26	—	0.33			I_{OL} = 5.2 mA
Input current	Iin	6.0	—	—	±0.1	—	±1.0	µA	Vin = V_{CC} or GND	
Quiescent supply current	I_{CC}	6.0	—	—	2.0	—	20	µA	Vin = V_{CC} or GND, Iout = 0 µA	

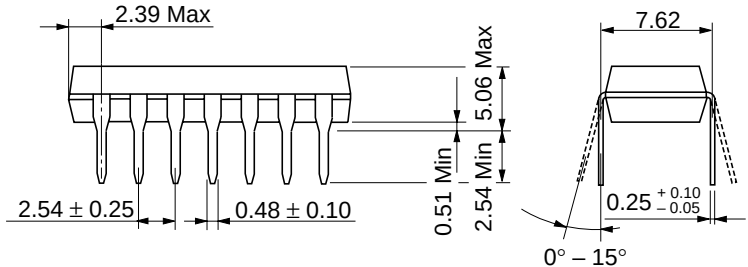
AC Characteristics (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

			Ta = 25°C			Ta = –40 to +85°C			
Item	**Symbol**	**V_{cc} (V)**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Maximum clock frequency	f_{max}	2.0	—	—	5	—	4	MHz	
		4.5	—	35	25	—	20		
		6.0	—	—	29	—	24		
Propagation delay time	t_{PLH} t_{PHL}	2.0	—	—	160	—	200	ns	Clock to Q or $\overline{Q}$
		4.5	—	14	32	—	40		
		6.0	—	—	27	—	34		
		2.0	—	—	160	—	200		Preset or Clear to Q or $\overline{Q}$
		4.5	—	13	32	—	40		
		6.0	—	—	27	—	34		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	Data to Clock
		4.5	20	1	—	25	—		
		6.0	17	—	—	21	—		
Hold time	t_h	2.0	5	—	—	5	—	ns	Clock to Data
		4.5	5	0	—	5	—		
		6.0	5	—	—	5	—		
Removal time	t_{rem}	2.0	25	—	—	31	—	ns	Preset, Clear to Clock
		4.5	5	–5	—	6	—		
		6.0	4	—	—	5	—		
Pulse width	t_w	2.0	80	—	—	100	—	ns	Clock, Preset, Clear
		4.5	16	8	—	20	—		
		6.0	14	—	—	17	—		
Output rise/fall time	t_{TLH} t_{THL}	2.0	—	—	75	—	95	ns	
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input Capacitance	Cin	—	—	5	10	—	10	pF	

Unit: mm

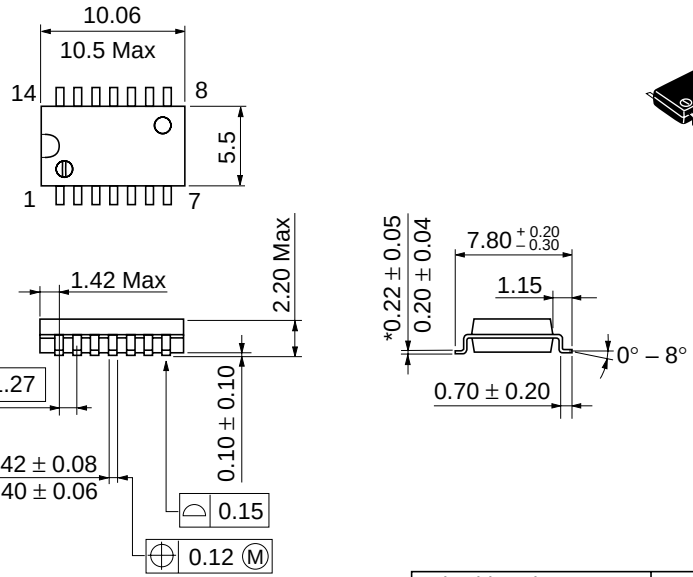


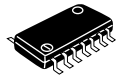




Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g

Unit: mm

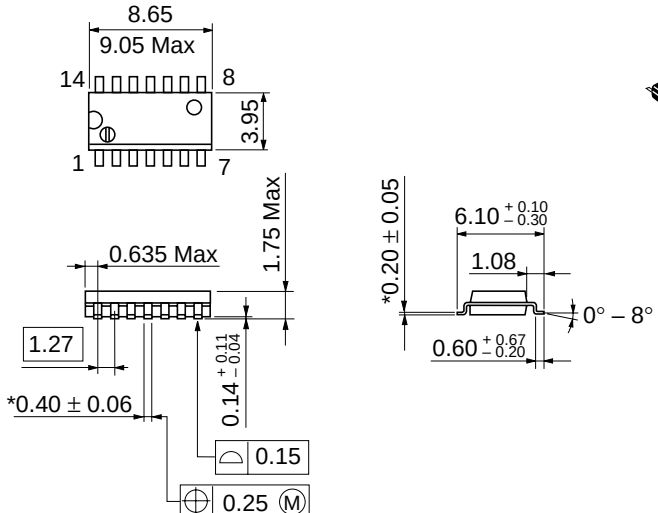




Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g

*Dimension including the plating thickness
Base material dimension

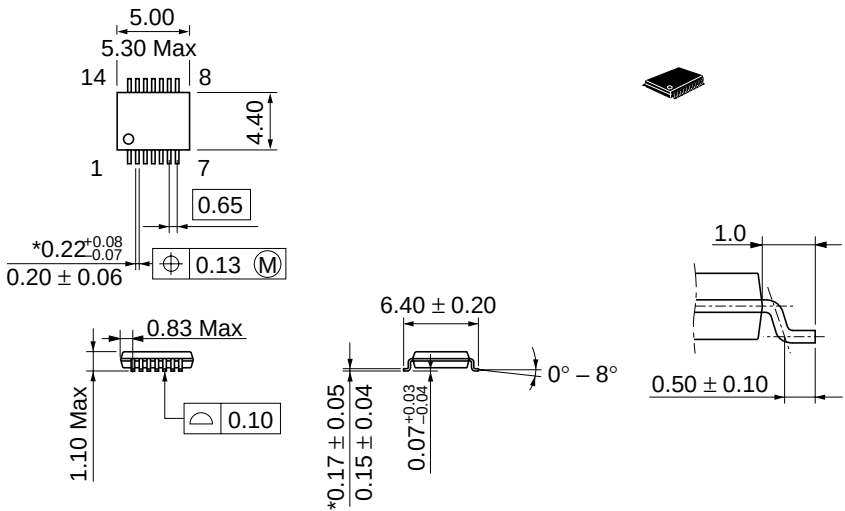
Unit: mm



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g

*Pd plating

Unit: mm



Hitachi Code	TTP-14D
JEDEC	—
EIAJ	—
Weight (reference value)	0.05 g

*Dimension including the plating thickness
Base material dimension

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